ON THE MODELING OF DUAL-MATERIAL DOUBLE-GATE FULLY-DEPLETED SILICON-ON-INSULATOR MOSFET

Ph.D. THESIS

by

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May 2011

To

My Parents

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CERTIFICATE

This is to certify that the thesis entitled **"ON THE MODELING OF DUAL-MATERIAL DOUBLE-GATE FULLY-DEPLETED SILICON-ON-INSULATOR MOSFET"** being submitted by **Alok Kumar Kushwaha** to the National Institute of Technology Kurukshetra, Deemed University, Kurukshetra for the award of the degree of **Doctor of Philosophy** is a record of bonafide research work carried out by him.

The matter presents in this thesis has not been submitted for the award of any other degree of this or any other institute.

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This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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ABSTRACT

Nowadays, the development of *VLSI* technology is mainly directed towards the miniaturization of semiconductor devices which in turn is heavily dependent on the advancement in the *CMOS* technology. The minimum dimension of a single device for present day technology is below *sub-100 nm* in channel length. As *CMOS* technology dimensions are being aggressively scaled down to the fundamental limits (such as reduction in carrier mobility due to impurity, increasing gate tunneling effect as the gate oxide thickness decreases, increasing p-n junction leakage current as the junction become more and more shallow, etc.) imposed by the material characteristics, secondary effects begin to influence the device performance significantly and more accurate device models as also innovative *MOS* device structures are required to be necessarily developed. These requirements have led to development of alternative technology. *Silicon-On-Insulator (SOI)* technology is one such alternative which can offer the performance as may be expected from next generation *Si* technology.

In this work, symmetric *Dual-Material Double-Gate Fully-Depleted SOI MOSFET* has been analyzed. The analytical model for the *MOSFET's* electrical parameters (such as potential distribution, electric field distribution, electron velocity distribution, subthreshold swing, threshold voltage, device capacitance, drain-current, transconductance, drain-resistance, cut-off frequency and transit time) has been developed and compared with the results for the device parameters obtained by numerical analysis using *ATLAS*. It has been observed that this structure provides for significantly improved electron transport efficiency and high frequency behavior of the device.

Since for obtaining optimal device performance, ion implantation is invariably used for doping the body region, the impurity distribution in the body region is assumed to be non-uniform. Also because, the accurate device models are required for designing *VLSI* circuits, the impurity distribution in the body region has been assumed to be Pearson IV distribution (rather than ideal Gaussian distribution function) which matches the implanted distribution very closely. The noise analysis (in analysis of thermal and flicker noise) of this proposed device has also been carried out and it has been observed that the proposed structure offers improved noise behavior.

A robust and fast neural network has also been developed which takes five major material/structural parameters of the *MOSFET* (namely silicon layer thickness (t_{si}), oxide layer thickness (t_{ox}), channel length ($L_g = L_1 + L_2$), drain-source voltage (V_{ds}) and gate-source voltage (V_{gs})) as inputs and gives five major device parameters (surface potential (ϕ_s), electric field distribution (E_x), drain-current (I_{ds}), transconductance (g_m) and cut-off frequency (f_c)) as outputs for a feasible *DM DG SOI MOSFET*. It can predict the output without going into complex analytical equations. In case the input parameters do not relate to a feasible device the neural network will not converge.

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List of symbols

$N_a(y)$	Impurity ion distribution
$\mu_n(x)$	Field dependent mobility of electrons
A_{011}, A_{022}	Arbitrary constants
V_{ds}	Applied drain-source bias
$A_i(x)$	Arbitrary function of x
V_{bi}	Built-in potential
v_{sat}	Carrier saturation velocity
r_{ds}	Channel resistance
g_m	Channel transconductance
a_i, b_i	Coefficients for silicon as target
E_c	Critical field
f_c	Cut-off frequency
C_d	Depletion layer capacitance
ε_{ox}	Dielectric constant of the oxide-layer
I_{ds}	Drain to source current
E_c	Electric field based on center potential
E_s	Electric field based on surface potential
χ_{si}	Electron affinity of silicon
q	Electron charge
$v_c(x)$	Electron velocity based on center potential
$v_s(x)$	Electron velocity based on surface potential
ϕ_F	Fermi potential
$g(y)$	Frequency function
V_{fbf1}	Front-channel flat-band voltages for M1
V_{fbf2}	Front-channel flat-band voltages for M2

L_g	Gate length
L_1	Gate length for metal M1
L_2	Gate length for metal M2
V_{gs}	Gate to source voltage
W	Gate-width
Q	Implant dose
C_{ss1}	Interface capacitance
N_{ss}	Interface state density
n_i	Intrinsic carrier concentration
$Q_n(x)$	Inversion layer charge
β	Kurtosis
μ_{no}	Low field mobility
$x_{d\max}$	Maximum depletion width
λ	Natural length
S_{vt}	Noise Power Spectral density
$E(x)$	Normal field
$h(y)$	Normalized distribution function
C_{ox}	Oxide layer capacitance
t_{oxb}	Oxide-layer thickness for back channel
t_{oxf}	Oxide-layer thickness for front channel
ε_{si}	Permittivity of the silicon film
ϕ_c	Potential at the center of the channel along *x*-axis
$\phi(x, y)$	Potential distribution in the *x, y* directions
ϕ_{B1}	Potential function along the back gate oxide-silicon interface under gate metal M1
ϕ_{B2}	Potential function along the back gate oxide-silicon interface under gate metal M2
$f(y)$	Probability density function
R_p	Projected range

I_{Dsat}	Saturated drain to source current
V_{dsat}	Saturated drain-source voltage
α	Scaling factor
E_g	Silicon band gap at 300 K
t_{si}	Silicon layer thickness
ϕ_{si}	Silicon work function
γ	Skewness
σ	Standard deviation
V_{sub}	Substrate potential
Q_d	Surface depletion charge
$Q_s(x)$	Surface layer charge
μ_s	Surface mobility
ϕ_{s1}	Surface potential under gate metal M1
ϕ_{s2}	Surface potential under gate metal M2
V_T	Thermal voltage
V_{th}	Threshold voltage
C_T	Total device capacitance
N_d	Total implant dose per unit area
τ	Transit time
W_m	Weighting matrix between the hidden and input layers
V_m	Weighting matrix between the output and hidden layers
ϕ_{M1}	Work function of gate metal M1
ϕ_{M2}	Work function of gate metal M2
$N_a\left(\frac{t_{si}}{2}\right)$	Doping concentration calculated at $y=\frac{t_{si}}{2}$
$S_{if}(f)$	Power spectral density of equivalent drain noise current
w_{nq}	Weighting value between the nth input neuron and the qth hidden neurons
B_{011}, B_{022}	Arbitrary constants

C_{VJ}	Vertical junction capacitance between the drain and substrate
C_{LJ}	Lateral junction capacitance between the side wall of the drain and the body
C_{VJB}	Capacitance of the buried oxide
C_{VJD}	Capacitance of the depletion region in the substrate below the *BOX*
E	Mean square error
$\boldsymbol{e}$	Vector of network errors
H	Hessian matrix
J	Jacobian matrix
k	Boltzmann's constant
$\boldsymbol{S}$	Subthreshold swing
S_d	Total number of data samples
T	Absolute temperature
C_{GS}	Gate-source trans capacitance
C_{SG}	Source-gate trans capacitance
C_{GD}	Gate-drain trans capacitance
C_{DG}	Drain-gate trans capacitance
C_{SS}	Source self capacitance
C_{DD}	Drain self capacitance

List of abbreviations

2D	Two Dimensional
3D	Three Dimensional
ANN	Artificial Neural Network
BOX	Buried Oxide
CMOS	Complementary Metal Oxide Semiconductor
DG	Double Gate
DIBL	Drain Induced Barrier Lowering
DM	Dual Material
DRAM	Dynamic Random Access Memory
FD	Fully Depleted
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
LM	Levenberg-Marquardt
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSE	Mean Square Error
nMOS	n-channel Metal Oxide Semiconductor
P IV	Pearson IV
PACE	Plasma Assisted Chemical Etching
PD	Partially Depleted
PDF	Probability Density Function
pMOS	p-channel Metal Oxide Semiconductor
RF	Radio Frequency
SCE	Short Channel Effects
Si	Silicon
SIMOX	Separated by Implanted Oxygen
SiO_2	Silicon dioxide
SM	Single Material
SOC	System On Chip
SOI	Silicon-On-Insulator

SRAM Static Random Access Memory

UFDG Ultra thin Fully Depleted Gate

ULSI Ultra Large Scale Integrated Circuit

UTB Ultra Thin Bodies

VLSI Very Large Scale Integrated Circuit

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List of publications

Papers published in International Journals

1. Alok Kushwaha, M. K. Pandey, S. Pandey and A. K. Gupta, **"Analysis of 1/f Noise in n-Channel Double-Gate Fully-Depleted SOI MOSFET",** International *Journal of Semiconductor Technology and Science*, Vol. 5, No. 3, pp-187-194, Sept.2005.

2. Alok Kushwaha, M. K. Pandey and A. K. Gupta **, "Pearson-IV type Doping Distribution based Analytical Modeling of Dual- Material Double-Gate Fully-Depleted Silicon-on-Insulator MOSFET (P-IV DM DG FD SOI MOSFET)",** *Microwave and Optical Technology Letters*, Vol. 49, No. 4, pp.979-986, April 2007.

3. Alok Kushwaha, M. K. Pandey, S. Pandey and A. K. Gupta **"Analytical Characterization of Drain Current, Transconductance and Channel-Resistance in Pearson-IV type Doping Distribution based Dual-Material Double-Gate Fully-Depleted SOI MOSFET"**, International *Journal of Semiconductor Technology and Science*, Vol. 7, No. 2, pp-110-119, June 2007.

4. Alok Kushwaha, M. K. Pandey and A. K. Gupta, **"Study of Flicker Noise in Dual-Material Double-Gate Fully-Depleted Double-Gate SOI MOSFET",** *IMSEC International Journal of Research*, Vol. I, No. 1, July-December, 2008.

5 Alok Kushwaha, M. K. Pandey and A. K. Gupta, **"Artificial Neural Network Model for n-Channel DM DG SOI MOSFET"** to *International Journal of Computational Intelligence: Theory and Practice,*(Communicated), June 2010.

Papers published in International/national Conferences

1. M. K. Pandey, S. Pandey, Alok Kushwaha and R.S.Gupta **"Effect of Implantation Profile on Design Aspects of Double Gate SOI MOSFET",** *International Workshop of Physics of Semiconductor Devices, Proc. IWPSD*, Chennai, pp. 570-572, 2004.

2. M. K. Pandey, Alok Kushwaha, P.J. George, S. Pandey and R.S. Gupta **"Analysis of Thermal Noise in Fully Depleted n-Channel Double Gate SOI MOSFET",** *Asia Pacific Microwave Conference*, *Proc. APMC*, Ashoka Hotel, N. Delhi, pp.915, 2004.

3. Alok Kushwaha, M. K. Pandey, S. Pandey and A. K. Gupta, **"An Artificial Neural Network Model for Thermal Noise in Fully depleted SOI-MOSFET"**, *National conference on Mathematical Techniques*, *Proc. MATEIT*, Delhi University, pp. 224-229, 2006.

4. Alok Kushwaha, M. K. Pandey, S. Pandey and A. K. Gupta, **"RF-Performance of Dual-Material Double-Gate Fully-Depleted SOI MOSFET with Pearson-IV type Doping Distribution**", *International Workshop of Physics of Semiconductor Devices*, *IWPSD,* IIT Bombay, Dec. 2007.

Chapter-I

INTRODUCTION

As the device count in an *IC* is running into billons per chip, the issue of power dissipation in the chip is becoming one of the two most important issues (other being the speed). The ever decreasing device dimensions have reached a state where the performance of the bulk *Si MOSFETs* is limited by the fundamental physical limits such as reduction in carrier mobility due to impurities, increasing gate tunneling effect as the gate oxide thickness decreases and increasing *p-n* junction leakage current as the junctions become more and more shallow. A low operating voltage is a necessity as reduced power consumption is aimed at. These requirements have led to development of alternative technologies. *SOI* technology is one such alternative which can offer a performance as expected from next generation *Si* technology.

Figure 1.1 shows the structures of *n*-enhancement bulk *Si MOSFET* and the corresponding *SOI MOSFET*. The main difference between the two is that the in *SOI* structure the *Si* layer containing the *MOSFET* is separated from the substrate by a layer of SiO_2, called buried oxide (*BOX*). The thin *Si* film on *BOX* is a crystalline layer. The typical dimensions of the layers are shown in the figure 1.1.

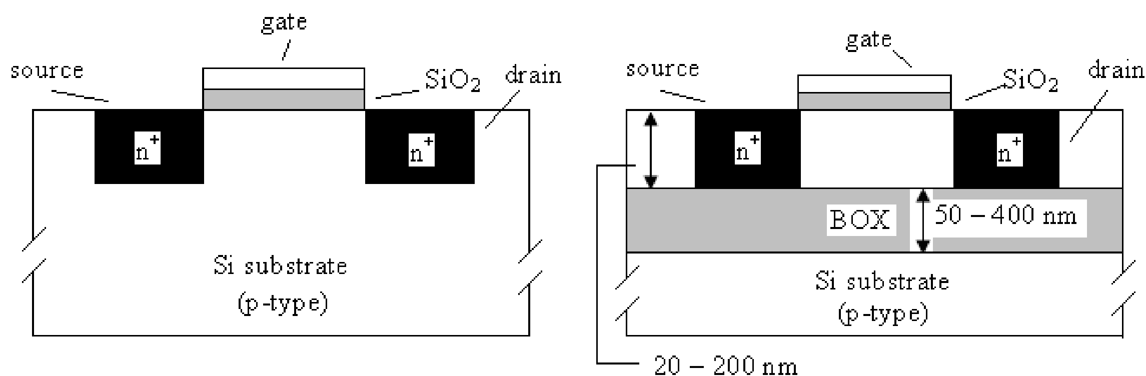

Fig 1.1 Structures of bulk Si MOSFET and SOI MOSFET.

1.1 Historical Perspective of SOI Development

In 1966, Watanabe and Tooi [1] observed that if oxygen ions are implanted into silicon using a *RF* gas discharge then the resulting SiO_2 has the characteristics identical to those of thermally grown SiO_2.

In 1978, it was discovered that if energy and dose of oxygen being implanted is kept *150 keV* and $12 \times 10^{18}\ cm^{-2}$ and the sample is annealed at a temperature of $1150^{o}C$, then the resulting buried oxide layer exhibits excellent electrical characteristics and the top *Si* layer is single crystal in nature. This process is known as *SIMOX* process, illustrated in figure 1.2.

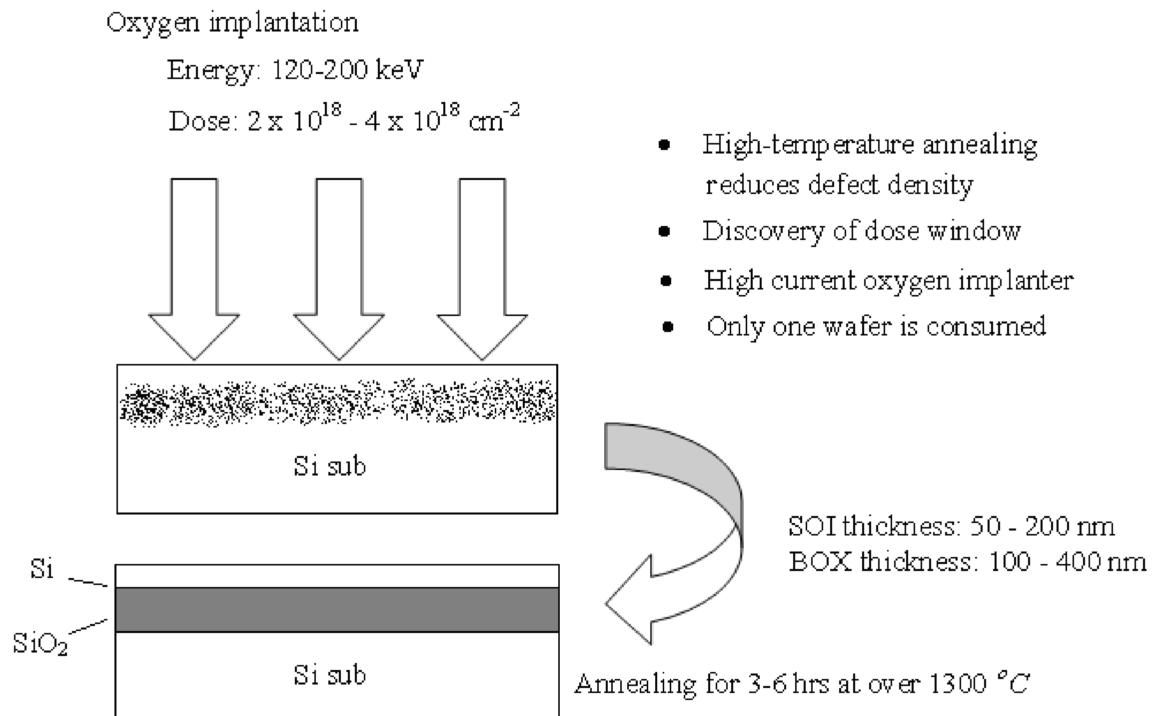

Fig 1.2 SIMOX process.

During 1980s, the recrystallization of *Si* layer with laser or *e*-beam was studied extensively and also formed a part of Japanese *R & D* project aimed at developing *3D ICs*. This project also included fabrication and evaluation of *SOI* substrates, design and simulation of *SOI* devices, and circuit design technology for *3D ICs* [2]. In the same tenure, there was an important improvement in *SIMOX* technology. It was discovered that if the annealing temperature is raised to above $1300^{o}C$, then the dislocation density is reduced from $10^{9}\ cm^{-2}$ to $10^{6}\ cm^{-2}$ [3].

During 90s, *SIMOX* process was further improved with the discovery of "dose window" [4] which resulted in drastic reduction in dislocation density and buried oxide thickness was increased by high temperature oxidation (*ITOX* technology) [5]. The resulting *SIMOX* technology led to increase in throughput by a factor of *5* and dislocation density as low as $10^2\ cm^{-2}$ to $10^3\ cm^{-2}$.

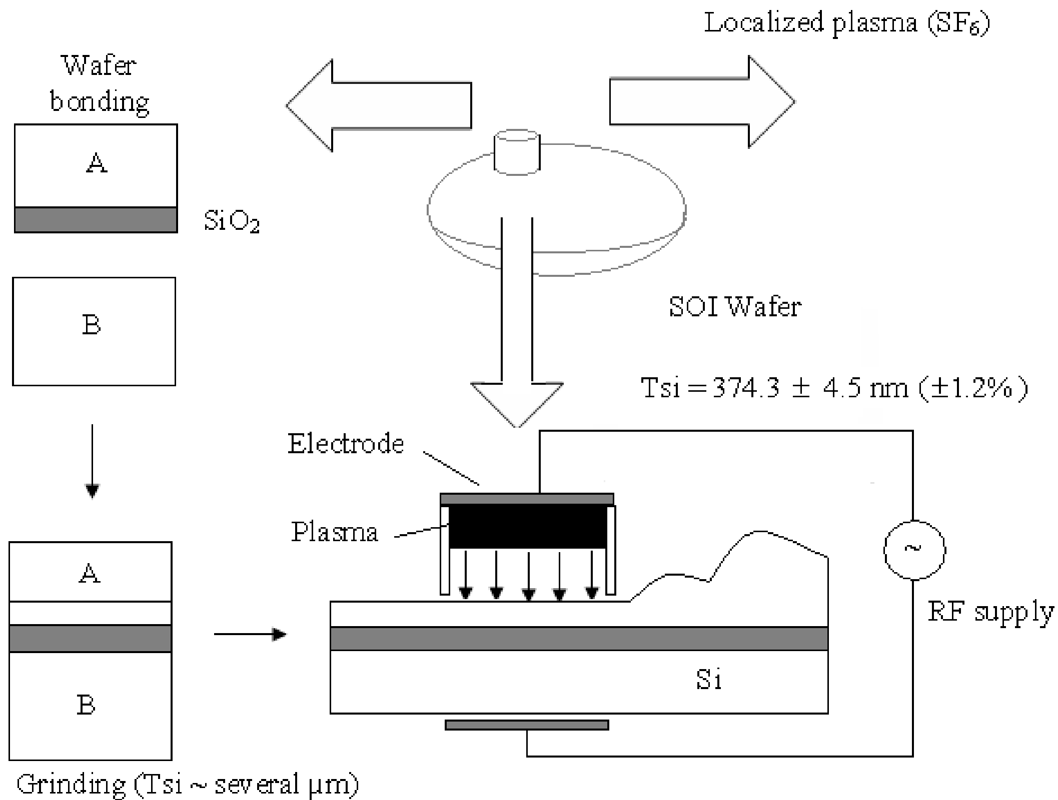

Fig 1.3 PACE process.

Since, the scaling of device dimension requires thinner and thinner top *Si* layer, considerable research efforts were made to develop *SOI* wafers with top *Si* layer having small but highly uniform thickness (thickness variation < 10%). As a result, plasma assisted chemical etching (*PACE*) process [6] and *ELTRAN* process [7] were developed in 1992 and 1994 respectively. The *PACE* process and *ELTRAN* is shown in figure 1.3 and 1.4 respectively.

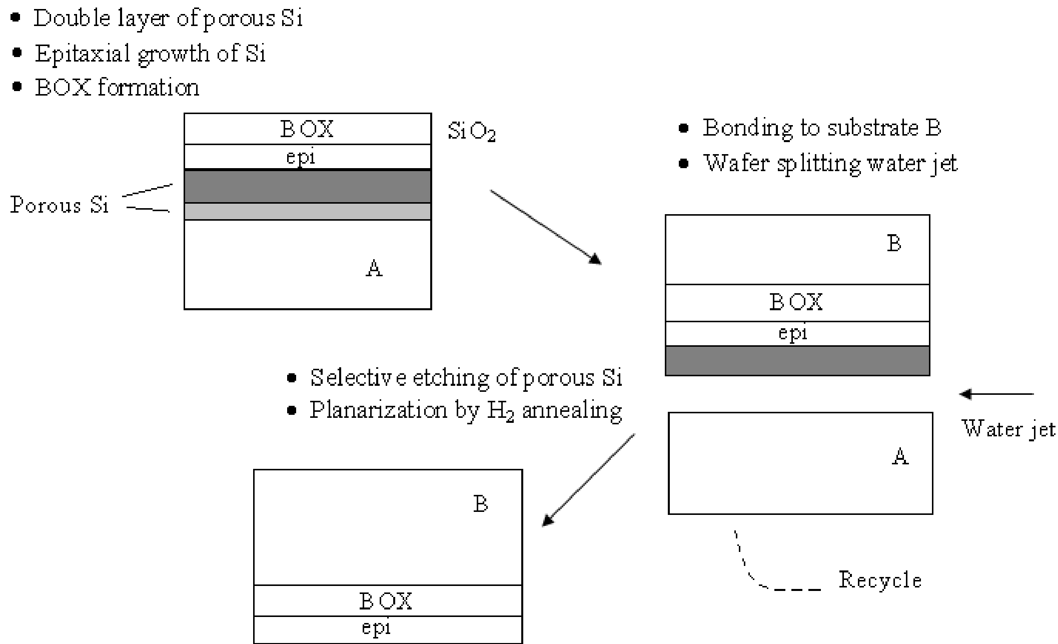

Fig 1.4 ELTRAN process.

In 1995, *UNIBOND* process with Smart-Cut technology was reported [8]. This process involved implanting hydrogen into a *Si* donor wafer, which is bonded to handle wafer. The donor wafer is split off at a temperature of 500^oC to 600^oC and a surface is planarized. The hydrogen dose required to strip the *Si* surface is from 3×10^{16} to 1×10^{17} cm^{-2}, which is less than the oxygen dose used for low-dose *SIMOX*. The donor wafer is recycled. The whole process is shown in figure 1.5.

A number of applications of *SOI* were developed at a commercial level. In the later half of 90s and onwards, the main applications developed are given below

1997 onwards →

- Gate Array (Mitsubushi)
- Power PC (IBM)
- MPC (Motorola)
- Watch Controller (Oki)
- Opteron (AMD) – 64-bit MDU
- CELL (Sony, IBM, Toshiba)

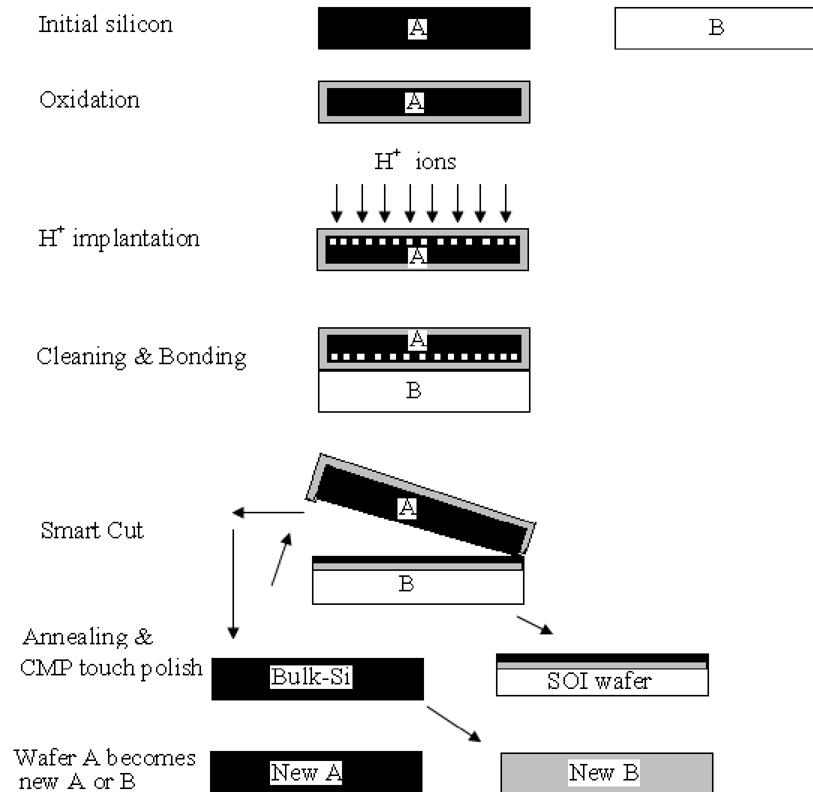

Fig 1.5 UNIBOND process.

1.2 SOI MOSFETs

1.2.1 Characteristics features

The main features of *SOI MOSFET* are listed below [2]

(i) Low drain junction capacitance: A schematic of cross sectional view of *SOI MOSFET* at the drain junction is shown in figure 1.6. The drain junction capacitance comprises of vertical junction capacitance between the drain and substrate (C_{VJ}), the lateral junction capacitance (C_{LJ}) between the side wall of the drain and the body. The component (C_{VJ}) is a series combination of the capacitance of the buried oxide (C_{VJB}) and the capacitance (C_{VJD}) of the depletion region in the substrate below the *BOX*. All these capacitances are shown in figure 1.6. Thickness of the body region is typically less than $0.1\ \mu m$, so the capacitance (C_{LJ}) is small. The vertical capacitances being in series resulting still smaller capacitance. Due to the above factor, overall drain junction capacitance in *SOI MOSFET* is much smaller than the same in bulk *MOSFET*. Typically, the drain junction capacitance for an *SOI MOSFET* is lower by one order of magnitude as

compared to the same in bulk silicon *MOSFET*, having same impurity concentration in the body. As a result of lower drain junction capacitance, the power dissipation during the switching of the transistor is less in *SOI MOSFETs*.

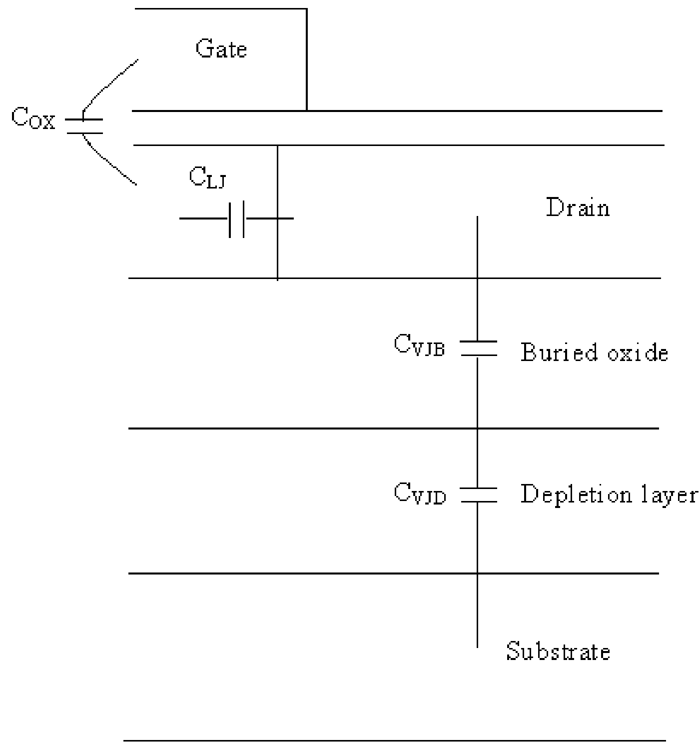

Fig 1.6 Drain Junction Capacitance of SOI MOSFET.

(ii) Improved speed of stacked gate: The body of *SOI MOSFET* is floating unless the layout is designed deliberately with a view to ground the body. In case of bulk *Si MOSFET*, where the body of both the pull-down transistor is connected to the ground (in case of *NAND* gate shown in figure 1.7), one of the pull down transistor has a negative body bias, due to the current flowing to the ground. This results in increase threshold voltage and higher fall time, in contrast if this *NAND* gate is implemented with *SOI MOSFETs*, the body bias becomes positive leading to lower threshold voltage, larger drain current and lower fall time (i.e. improved speed).

(iii) Ideal device isolation: *SOI* devices are laterally isolated from each other by oxide (shallow-trench-isolation) and vertically by *BOX*. Since *SOI* is an excellent insulator, *SOI MOSFET* structure provides for near ideal device isolation.

(iv) Radiation hardness: Alpha particles generated by trace amount of radio active

elements typically have energy of *5 MeV*. These particles can penetrate the *Si* up to a depth of *25 μm* generating excess electron-hole pairs on the way. The excess electron-hole pairs are sufficient to change the memory states of a *SRAM*. In *SOI MOSFETs* most part of the trajectory of the alpha particle is below the *BOX* and the electron-hole pairs generated in the substrate are electrically isolated from the active region of the device. Thus *SOI MOSFETs* are relatively immune to the radiations effect.

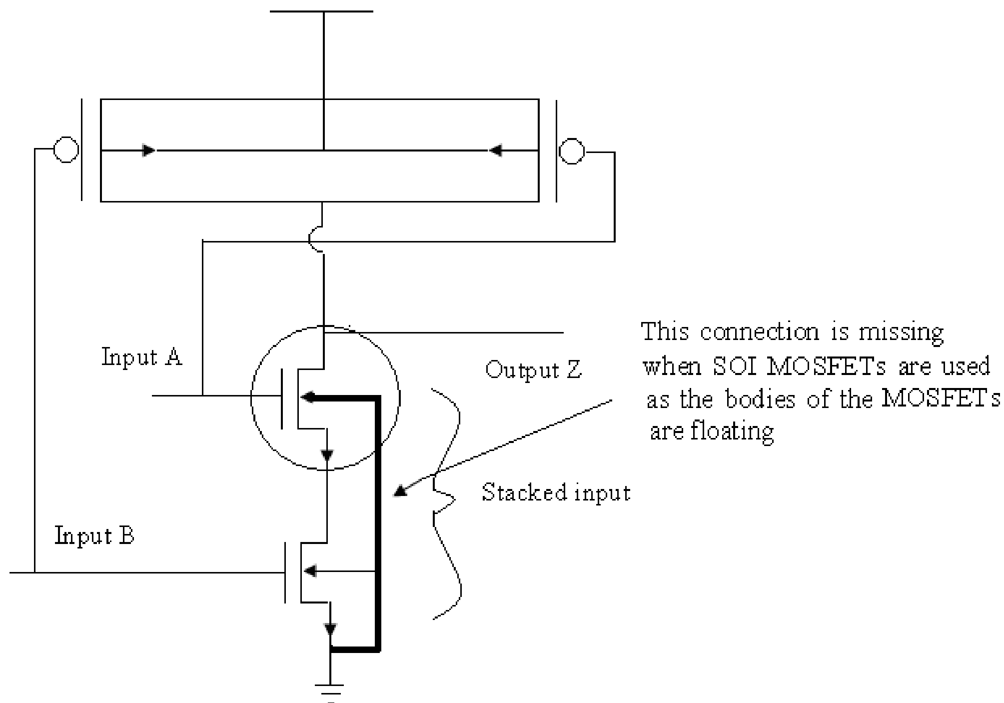

Fig 1.7 Higher speed of the stacked gates with the SOI MOSFETs.

(v) <u>Small *p-n* junction leakage current</u>: The *p-n* junction leakage current in *SOI* structure is very small because the effective area of the *p-n* junction besides the side wall area which is small due to the small thickness of the top silicon layer. This leads to low standby power requirement.

(vi) <u>Reduced short-channel effects</u>: Because the thickness of the body layer and therefore the depth of source-drain junction in *SOI MSOFET* is very small, so the short channel effects are greatly reduced even for small channel length.

(vii) <u>No latch-up</u>: Latch-up in *CMOS* structures implemented in bulk *Si* device occurs due to parasitic thyristor as shown in figure 1.8 (a). This phenomenon limits the maximum operating voltages and necessitates special circuit layout to prevent latch-up.

In case of *SOI CMOS* there is no parasitic thyristor (see figure 1.8(b)) and therefore it is free from latch-up phenomenon.

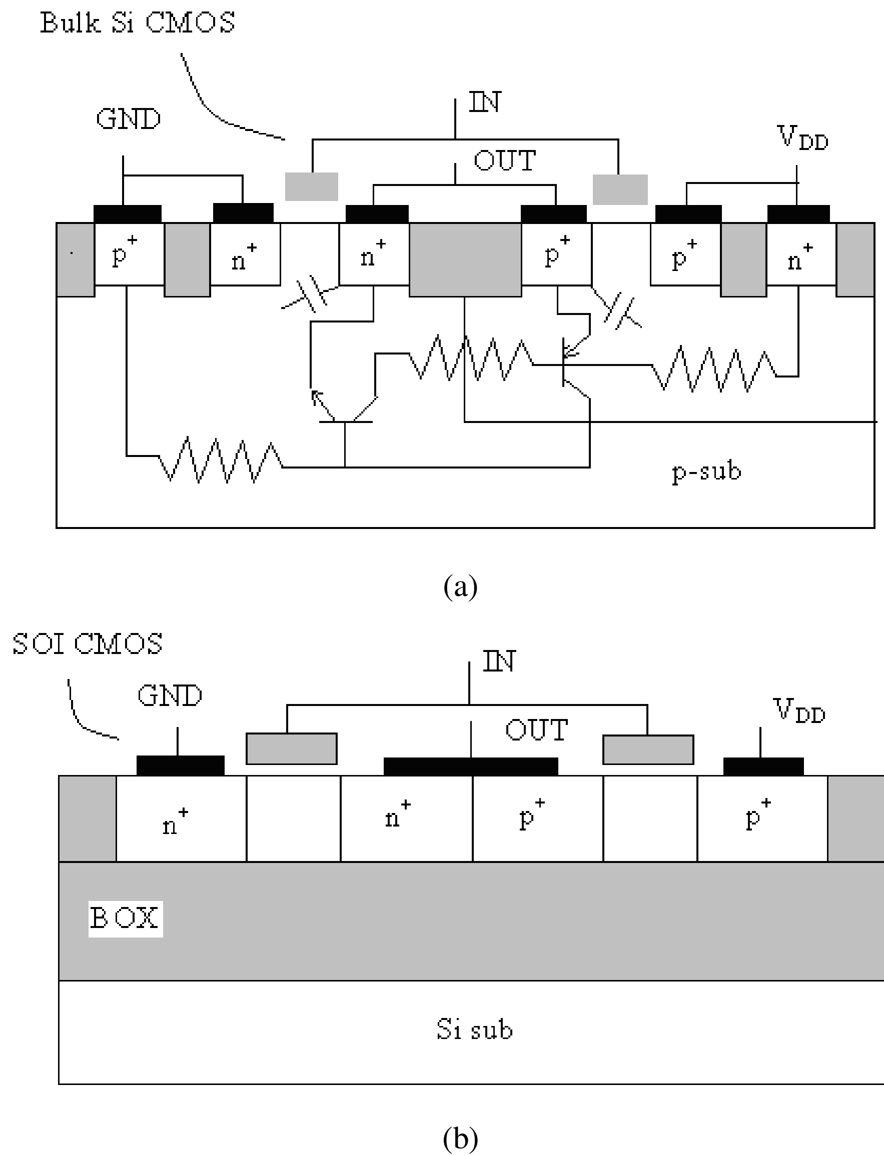

Fig 1.8 Latch-up in CMOS.

1.2.2 Operating Modes of SOI MOSFETs

(a) Partially-depleted (*PD*) vs Fully-depleted (*FD*): Figure 1.9 shows the schematic cross section view of *PD* and *FD SOI MOSFETs*.

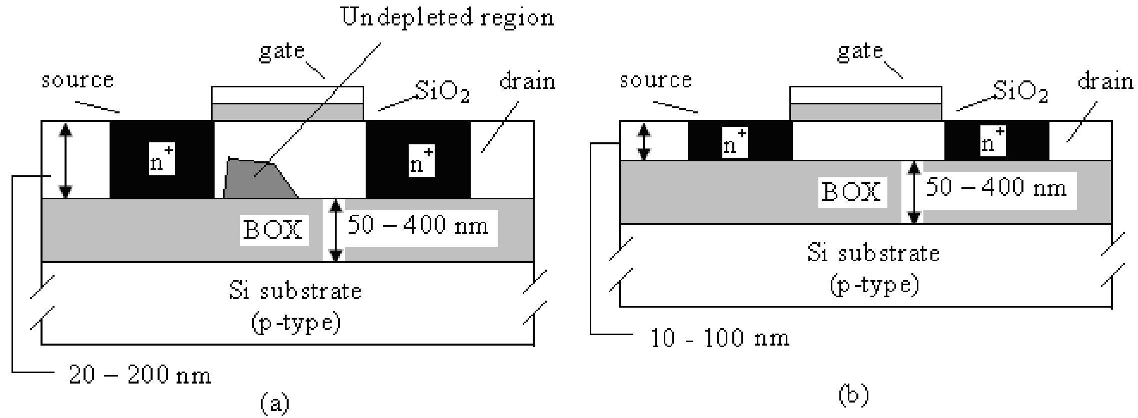

Fig 1.9 Structures of (a) Partially-Depleted and (b) Fully-Depleted SOI MOSFET.

In *PD MOSFET,* a part of the body region remains undepleted or neutral while in *FD MOSFET,* whole of the body, the depletion region extends right up-to the body and *BOX* interface. Thus in *FD SOI MOSFET,* the complete body region is depleted off majority carriers.

(b) Comparison of *PD* and *FD SOI MOSFETs*: The characteristics of *PD* and *FD MOSFETs* differ in the following respects [2].

(i) Kink in the drain current characteristics: In *PD SOI MOSFETs*, a kink (sharp rise in drain current at a particular drain voltage) is observed in the I_D vs V_{DS} characteristics as the drain voltage is increased for a fixed gate voltage. As in *n*-channel *MOSFETs* as the electrons flow towards the drain they gain kinetic energy and generate electron-hole pairs by impact-ionization. The holes so generated moves towards the source. In *PD SOI* device there is higher potential barrier to the holes so the hole tend to accumulate in the body region thereby increasing the body voltage. This causes threshold voltage to drop, drain current to increase leading to even higher impact-ionization. At the same time barrier height for holes also decreases permitting more number of holes to reach the source thereby increasing the drain current. This results in sharp increase in the drain current (a kink) at some drain voltage. To avoid this kink the body of *PD SOI MOSFETs* needs to be connected to ground. In *FD SOI* devices, the potential barrier to the hole at the source end is small because whole of the body region is depleted of the carriers. So, there is no accumulation of holes in the body region and consequent kink in the drain characteristics.

(ii) Subthreshold slope: An important feature of *FD SOI MOSFET* is that they have steep subthreshold behavior characterizes by subthreshold swing close to *60 mV/decade* which is limiting value for *MOSFETs*. The subthreshold behavior of *PD SOI* is similar to bulk *Si MOSFETs*. Thus subthreshold characteristics of *FD SOI MOSFETs* are superior.

(iii) Dynamic floating body effects: As mentioned above, the *SOI* devices are fully isolated and their body potential is not constant. The effects of different body potential are collectively known as floating body effect. Dynamic body floating effects refer to the device behavior when it is operating in a circuit. The body potential changes because of impact-ionization in majority redistribution in the body region when gate and drain switch between high and low levels. *FD SOI* devices are stable and relatively unaffected by the dynamic body effects. In contrast the *PD SOI* devices are significantly sensitive to dynamic body effect and require the body to be connected to a constant potential. These floating body effects have been known to cause the transient phenomenon in the access transistor of *DRAMs* and *SRAMs* that can lead to loss of charge in memory cell [9].

(iv) Parasitic bipolar effects: In *FD SOI MOSFET*, a parasitic bipolar transistor is formed where source, body and drain act as emitter, base and collector respectively of parasitic transistor. In this transistor, base current is consist of majority carriers, generated by impact-ionization. Since the body region is more depleted in *FD* than *PD SOI* device. The parasitic transistor is more effective in *FD SOI* devices. This transistor leads to a reduction to breakdown voltage between the source and drain, smaller threshold voltage and abnormally steep subthreshold behavior. This parasitic effect may also lead to single transistor latch phenomenon [10]. The parasitic bipolar effect can be suppressed by suppressing the generation of majority carrier by impact-ionization, reducing the injection efficiency of the parasitic bipolar transistor and by lowering the transport efficiency in the base of the transistor.

(v) Self heating effect: Self heating effects are common to both *PD* and *FD SOI* devices. The *BOX* layer which leads to better characteristic of the device is also responsible for its poor thermal behavior. The oxide has a thermal conductivity which is two orders of magnitude smaller than that of silicon. So, the heat generated by the drain current is not able to escape through the *BOX* layer and has to be dissipated by the

interconnections via the contact of source, drain and gate. This may results in increase in channel temperature and consequent degradation device behavior.

1.3 State of Art – FD SOI MOSFETs

1.3.1 Fully-Depleted SOI MOSFET Structures

Due to the superior characteristics of *FD SOI* devices, considerable effort has been invested in recent years leading to innovative device structures in the quest of better performance. These devices have been classified as non-classical by *ITRS* (International Technology Roadmap for Semiconductors). Figure 1.10 illustrates the evolution of *FD SOI* devices from single-gate to multi-gate structures.

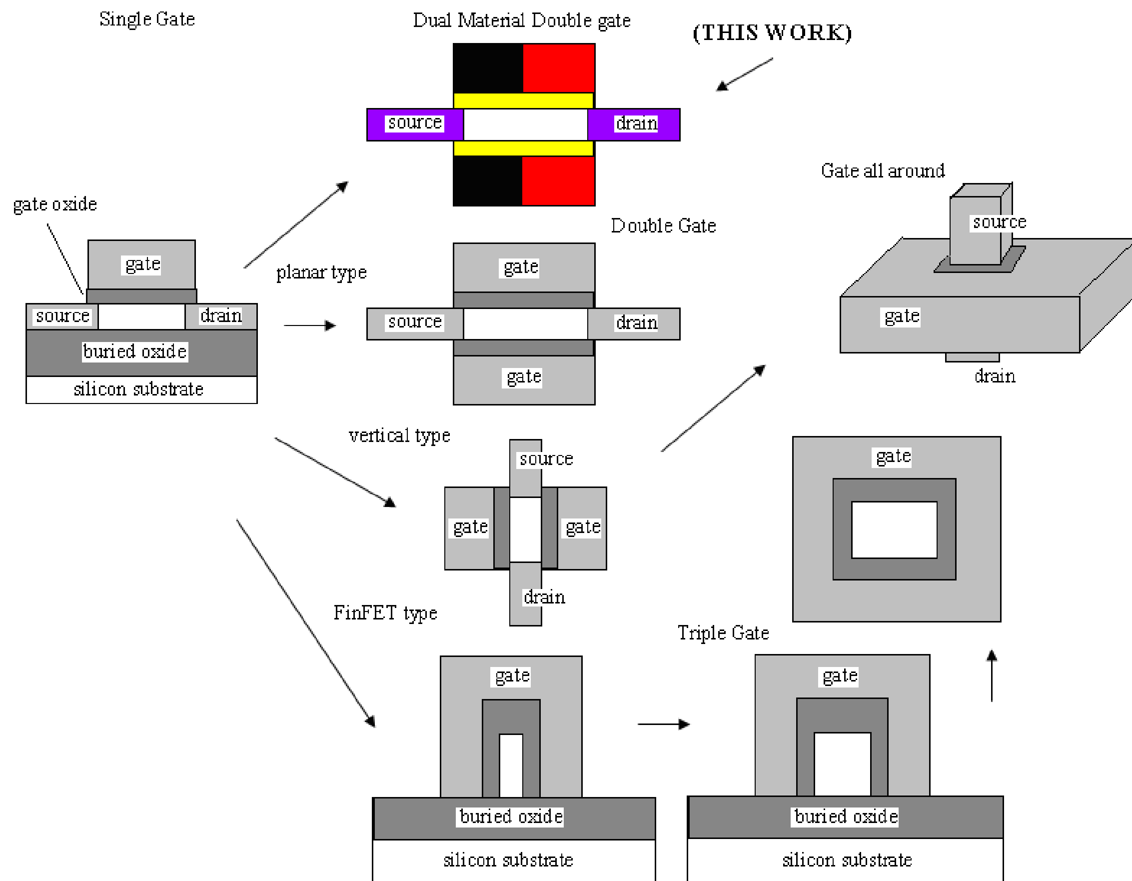

Fig 1.10 Evolution of FD-SOI devices from single-gate to multi-gate structures [11] – [25]. [68]

In single-gate structures, the gate length must be more than four times the thickness of the *SOI* layer to suppress the short channel effects. Double-gate and triple-gate *MOSFETs*

have relatively smaller short channel effects, so the gate length can be as small as twice the thickness of *SOI* layer. Double-gate structures with one gate consisting of dual-material [26] have also been analyzed. Both gates consisting of dual material (**this work**) have been proposed, also illustrated in figure 1.10. Triple-gate devices give somewhat better characteristics because three-gates allow better control of channel potential. Gate all around devices have more complicated structure and are difficult to fabricate. *FinFET,* double and triple-gate are more promising alternatives for nano-scale devices.

1.3.2 Double-Gate FD SOI MOSFETs – a brief review

Double-gate *SOI MOSFET* has two gates simultaneously controlling the charge in the thin silicon body layer, allowing for two channels for current flow. Because *SOI* film is thin, a direct charge coupling exists between the front and back gate invariably [27], influencing the terminal characteristics of the device. The device can be operated in several ways [28]:

- Front channel alone conducting, the back channel being either depleted or accumulated.
- Both channels conducting, both or either of the channels being in weak or strong inversion.

The current-voltage characteristics of the device with the front channel in strong inversion and the back channel either in accumulation or in depletion has been modeled analytically [29]-[31]. Since *SOI* films are thin, the electrical properties of *MOSFETs* fabricated are inherently influenced by the charge coupling between the front and back gates. Due to extremely small device dimensions, low voltage operation will be mandatory where the low threshold voltage is required [32]. Sasaki and Togei [33] studied the variations in the threshold voltage of *SOS* (silicon on sapphire) *MOSFET* as a function of epitaxial film thickness. Worly [34] derived an analytical model for the threshold voltage of an *SOS* transistor in which charge coupling between the front and the back gates occurs as in *SOI MOSFET*, but only the back silicon surface is depleted. Sano et. al. [35] developed a rigorous numerical model for threshold voltage (V_{th}) that includes a dependence on the back gate bias. A general steady state analysis of charge coupling

between the front and back gate that yielded closed form expressions for V_{th} under all possible steady state charge conditions was presented by Lim and Fossum [27]. They also discussed the dependence of the linear region channel conductance on the back gate bias and other device parameters.

Both *n*-type and *p*-type *SOI MOSFET* structures were considered by Ballestra et. al. [36]. They analyzed the effect of the interface parameters on the back and the front threshold voltages. Groeseneken [37] studied the temperature dependence of the threshold voltage of the ultra thin *SOI n*-channel *MOSFET*. The threshold voltage variation with temperature is significantly smaller in fully depleted devices than in bulk devices. In this paper, the dependence of V_{th} on the depletion level was also discussed. The statistical variation of V_{th} resulting from the randomness in impurity distribution in both bulk and *SOI MOSFET* was discussed by Chen and Li [38]. Their study revealed that the threshold voltage of *DG FD SOI MOSFET* is less sensitive to inherent fluctuations in impurity distribution and discussed the design considerations for minimizing the statistical variation in V_{th}. Over the past thirty years, the primary challenge for the *IC* designers has been the integration of an ever increasing number of devices with high yield and reliability. However, as the device dimensions approach deep submicron regime, the characteristics of a conventional *MOSFET* approach that of a resistor [39]. Increasing the threshold voltage through increased channel doping solves this difficulty. However, this would require higher supply voltage and also result in higher capacitance. This combination would result in higher power dissipation and low speed which are undesirable. So a tradeoff is required. Based on Brews empirical scaling rule [40], Yan et. al. [41] has proposed the guidelines for the design of *SOI MOSFETs*. They discussed several structural variations of conventional *SOI* structure in terms of natural length scale to guide the design.

The requirement of low voltage operation made the investigations of subthreshold characterization important. The subthreshold behavior of a *MOSFET* is characterized by the subthreshold swing, which has to be small enough to ensure low leakage current and sufficient overdrive necessary for high speed. The dependence of the subthreshold swing (***S***-factor)* on current capability of the *MOSFET* has been discussed for the gate length down to $0.1\ \mu m$ [42]. In the subthreshold region, the floating body (of *FD SOI* device)

leads to a shift in the subthreshold slope which is smaller than the theoretical value of $60\ mV/decade$ predicted for an ideal *MOS* transistor at room temperature. Davis et. al. [43] observed subthreshold slope as small as $50\ mV/decade$ for *n*-channel *MOSFETs* fabricated on *SOI* substrate. Advances in *SOI* wafer technology have improved the material quality substantially leading to *n*-channel *MOSFET* subthreshold slope of less than $20\ mV/decade$ [44]. Good understanding of this subthreshold behavior of floating body *SOI MOSFET* is necessary for proper transistor design and circuit modeling. Previously reported ***S***-factor models [45]-[48] are based on one-dimensional analysis of the *SOI MOSFET* and cannot be applied to short channel devices where the potential distribution is essentially two dimensional. Two-dimensional analysis of subthreshold behavior using numerical analysis approach has been reported in [49]-[50] for *DG FD SOI* devices.

Matloubian et. al. [51] showed that *n*-channel *SOI MOSFETs* with floating bodies show a threshold voltage shift and improvement in subthreshold slope at higher drain biases. This improvement was supported by the positive feedback between the body potential and the transistor channel current. Subthreshold slopes in submicron *n*-channel *FD SOI MOSFETs* have been measured as a function of substrate bias and temperature as well as drain bias by Tokunaga et. al. [52]. It was found that for low drain voltage, a simple capacitor model could explain the experimental results. For large drain voltages anomalously sharp subthreshold characteristics was observed for large negative substrate biases. They also proposed a qualitative model based on the charge state of the lower *SOI* interface to explain the dependence of the anomalous effect on substrate bias. The model for current-voltage characteristics in subthreshold region for submicrometer fully-depleted *SOI-MOSFET* was proposed by Fossum [53] and Hasio [54].

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* Subthreshold slope or ***S***-factor is defined as $\boldsymbol{S} = \dfrac{1}{(\partial \log(I_D)/\partial V_G)}$

The above slope is computed for I_D vs V_G curve in subthreshold region with V_{DS} kept as constant.

The model for current-voltage characteristics in subthreshold region for submicrometer fully-depleted *SOI-MOSFET* was proposed by Fossum [53] and Hasio [54]. Fossum, et. al. [53] observed the abnormally large drain current in subthreshold region and related it to the floating body effects due to the impact-ionization at the drain. Hasio et. al. [54] proposed the analytical model for subthreshold current voltage characteristics taking into account the dependence of effective depletion charge on the drain bias and the voltage drop in the substrate region underneath the buried oxide. Short channel effects like threshold voltage roll off and drain induced barrier lowering were also analyzed for a gate length up to $0.25\ \mu m$.

Based on the analysis of Ratnakumar and Meindl [55], Woo et. al. [56] separated the *2D* Poisson's equation into a one-dimensional Poisson's equation and *2D* Lapalace equation. To solve the *2D* Poisson's equation Green's function technique can also be applied as demonstrated by Lin and Wu [57] for a bulk *MOSFET* and by Chin and Wu [58] for a short channel length *MESFET*. The exact solution of the *2D* Poisson's equation for the fully depleted *SOI MOSFET* has been derived using three zone Greens function technique by Gou and Wu [59].

A symmetric dual-material dual-gate *MOSFET* structure has been analyzed by Manoj Saxena [60] and in their work a *2D* analytical model was developed for potential and electric field distribution in the body region and the threshold voltage assuming uniform distribution in the body region. Asymmetric *DM FD SOI MOSFET* has also been analyzed by Anurag Chaudhry and M. Jagadesh Kumar [61, 26] assuming uniform distribution in the body region.

Keunwoo Kim, and Jerry G. Fossum [62] presented asymmetrical double-gate (*DG*) *CMOS*, utilizing n+ and p+ polysilicon gates, can be superior to symmetrical-gate counterparts. The most noteworthy result was that asymmetrical *DG MOSFETs*, optimally designed with only one predominant channel, yield comparable, and even higher drive currents at low supply voltages.

Adelmo Ortiz-Conde et al. [63] offered an explicit analytic solution of the surface potential of undoped-body symmetric dual-gate devices. The error produced by the proposed solution compared to exact results is reasonably small for typical device dimensions and bias conditions.

1.3.3 Performance Characteristics of DG, SG MOSFETs and others

Wei Ma and Savas Kaya [64] measured the impact of device physics on **double-gate**, **silicon-on-insulator** and **bulk metal oxide field effect transistor** as shown in figure 1.11, in terms of drain current, transconductance and output conductance. It was observed that:

- Drain current, so as the transconductance is high in case of *DG* as compared to *SOI* and bulk *MOSFET*, as shown in figure 1.11 (a) - (b).
- Also g_d reduces more rapidly in *SOI* and *DG MOSFETs*, which have a thinner active *Si* layer, hence a lower output conductance. For V_{ds} > 0.5 V, g_d remains relatively flat in *SOI MOSFET*, while *DG* and bulk *MOSFETs* have comparable response, except lower value of g_d in the former case, as shown in figure 1.11 (c).

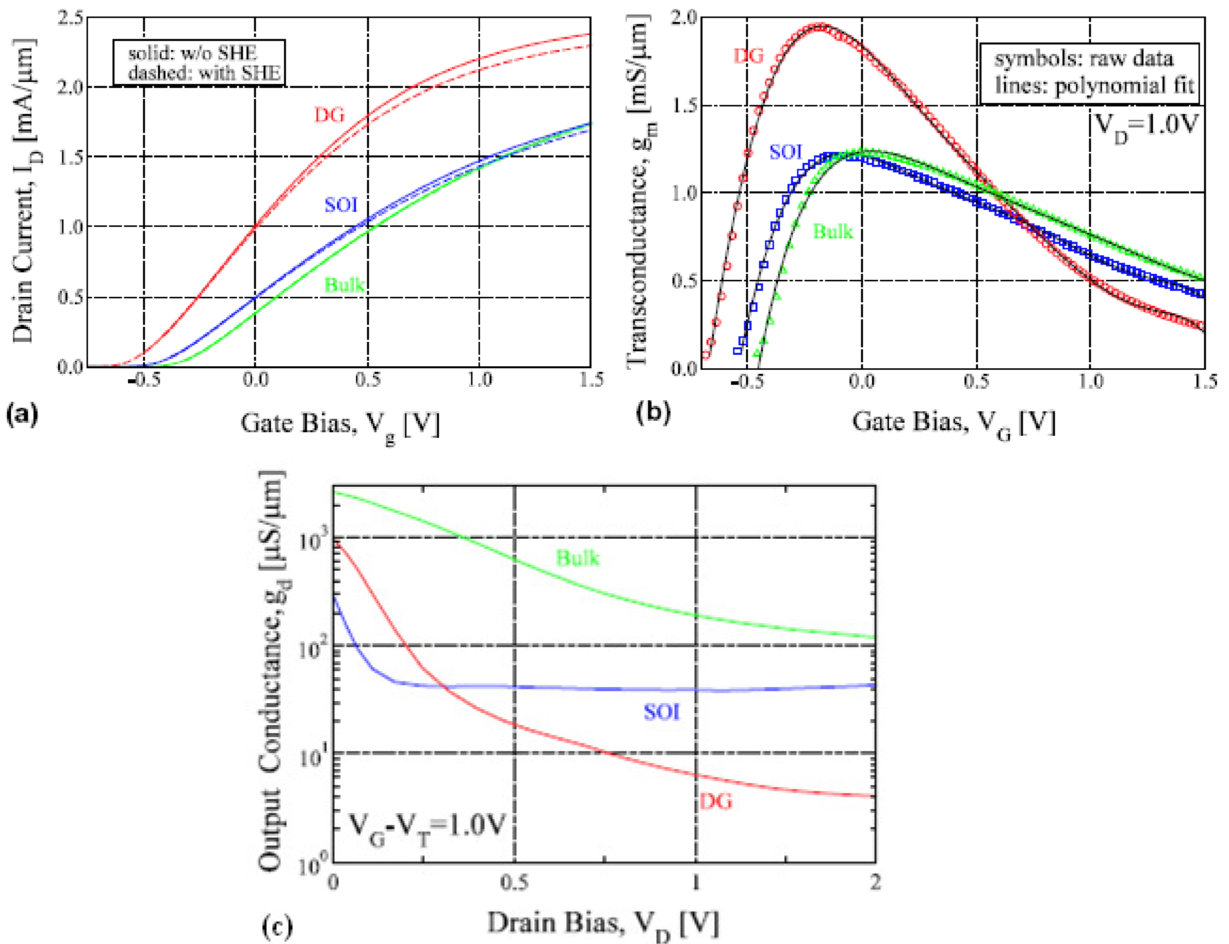

Fig 1.11 (a) I_d–V_g characteristics (b) Corresponding transconductance curves for the same devices (g_m) (c) Drain-bias dependence of g_d is typically low in saturation but non-zero. Source: Wei Ma and Savas Kaya [64]

Julie Widiez et. al.[65] proposed *DG MOSFETs*, with gate lengths down to 40 nm, and experimentally compared to *SG* and *GP* (ground plane) *MOSFETs*. It was observed that the *DG* transistor shows the best *SCE* control and performance. Some of the performance outcomes are given below:

- *DG* transistors exhibit the best electrical results in terms of *SCEs* and saturation currents for both *nMOS* and *pMOS* transistors, as shown in figure 1.12.
- *DG* devices exhibit a low symmetrical threshold voltage V_{th} adjusted to 0.45 V. Conversely, the *GP* architecture shows a very high threshold voltage due to the influence of the grounded back gate, as shown in figure 1.13.

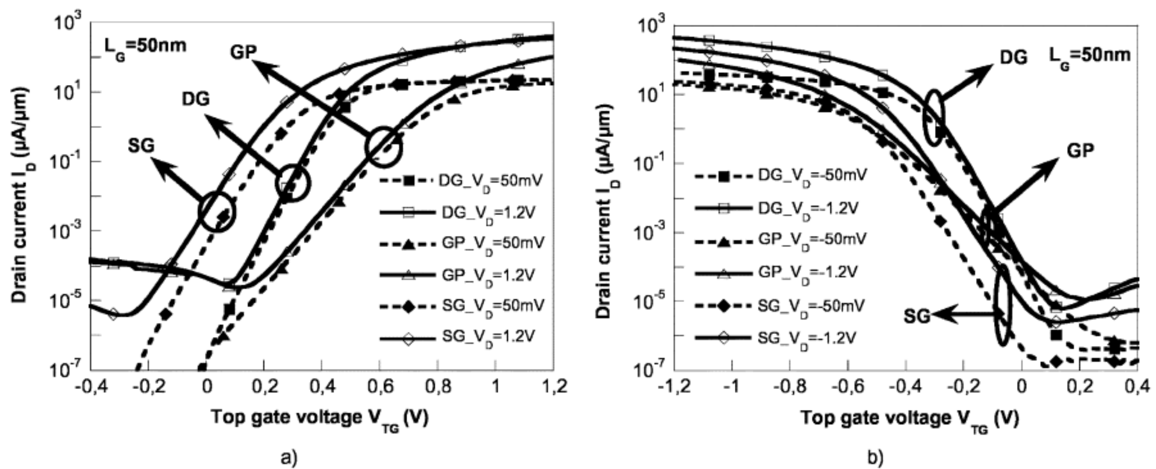

Fig. 1.12 Drain current versus gate voltage for SG, DG, and GP (Ground Plane) transistors with a gate length of 50 nm for both (a) nMOSFETs and (b) pMOSFETs. Source: Julie Widiez et. al.[65]

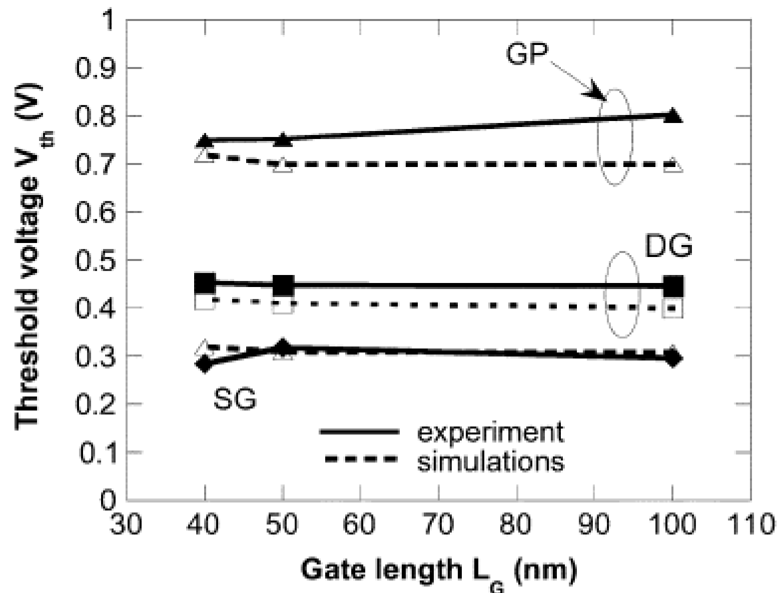

Fig. 1.13 Threshold voltage as a function of the gate length at V_{ds} = 50 mV for nMOS devices. Dashed lines are simulations. Source: Julie Widiez et. al.[65]

- The drive and off-state currents (respectively I_{on} and I_{off}) extracted at $V_{ds}=-1.2V$. As expected, *DG MOSFETs* exhibit the highest saturation current, whereas *GP* transistors show a lower current due to their higher threshold voltage, as shown in figure 1.14.
- *GP* transistors are almost as good as *DG* transistors, whereas *SG* device exhibits higher values of *DIBL*, because of the *1.2 μm* thick *BOX*, as shown in figure 1.15.

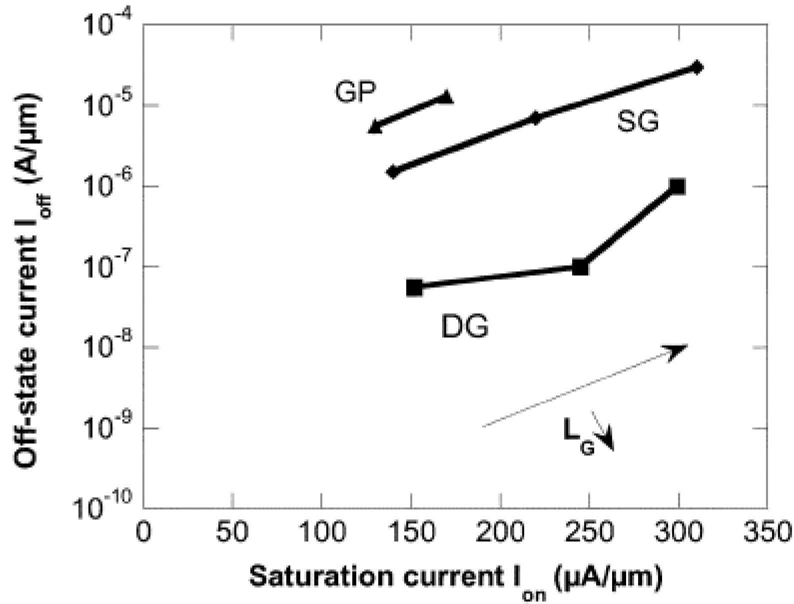

Fig. 1.14 Off-state current (I_{off}) versus saturation current (I_{on}) for pMOS transistors with different gate lengths. Source:Julie Widiez et. al. [65]

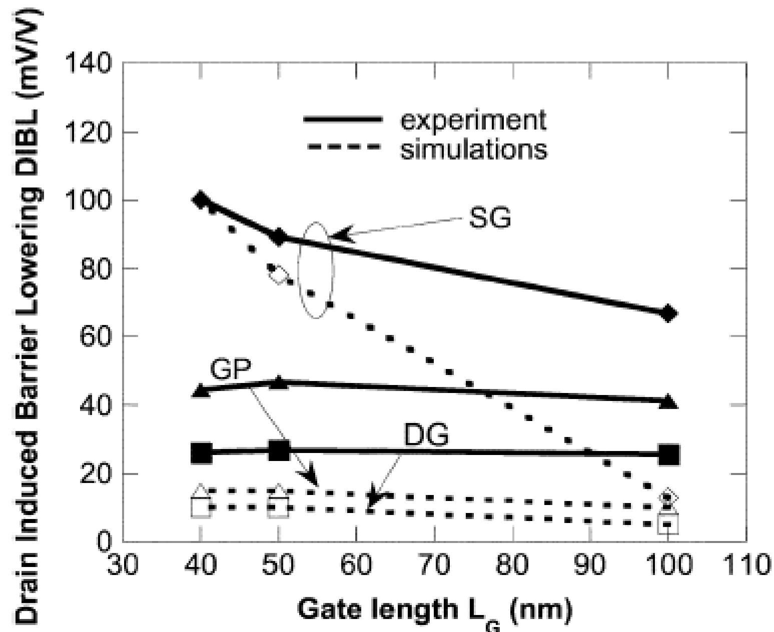

Fig. 1.15 DIBL versus gate length (L_g) for nMOS devices. Dashed lines are for simulations. Source: Julie Widiez et. al.[65]

- Values of V_{th}, ΔV_{th}, S, I_{on}, I_{off} and μ_o are compared for *DG, GP* and *SG* in table 1.0.

Table: 1.0 Comparison of DG, GP and SG MOSFETs. Source: Julie Widiez et. al.[65]

parameter	transistor	Double Gate	Single Gate	Ground Plane
V_{th}	nMOS	0.45V	0.3V	0.8V
	pMOS	-0.45V	-0.65V	-0.77V
ΔV_{th}	nMOS	0	25mV	50mV
	pMOS	163mV	226mV	252mV
S	nMOS	64mV/dec	80mV/dec	104mV/dec
	pMOS	66mV/dec	122mV/dec	130mV/dec
μ_0 (cm^2/Vs)	nMOS	212	146	50
	pMOS	51	55	28
I_{on} (µA/µm) (V_D=V_G=-1.2V)	pMOS	506	346	145
I_{off} (A/µm) (V_D=-1.2V, V_G=0V)	pMOS	$4.3\ 10^{-9}$	$8.3\ 10^{-7}$	$4.1\ 10^{-9}$

M. Jagadesh Kumar and G. Venkateshwar Reddy [66] observed the diminished short channel effects in **nanoscale double-gate silicon-on-insulator metal oxide field effect transistor** due to Induced Back-Gate Step Potential in which the front gate consists of two materials with different work functions, as shown in figure 1.16. It has been observed that:

- *DM DG* structure exhibits a step in the surface potential profile, as shown in figure 1.16 (a), at the front gate as well as at the back gate. The step, which is quite substantial in the front gate surface potential, occurs because of the difference between the work functions of n+ poly and p+ poly).
- The back gate surface potential profile plays a dominant role in deciding the threshold voltage of an asymmetrical *DG SOI MOSFET* and due to the presence of the induced step profile at the back gate, the short channel behavior of this structure is expected to improve, as shown in figure 1.16 (b).

- The threshold voltage decreases with smaller channel lengths for the *DG* structure while a threshold voltage roll-up can be observed for the *DM DG* structure, as shown in figure 1.16 (c).
- *DIBL*, which is the difference between the linear threshold voltage ($V_{th,lin}$) and the saturation threshold voltage ($V_{th,sat}$) is far less for *DM DG* structure when compared with that of the *DG* structure, as shown in figure 1.16 (b). The reduced *DIBL* in the *DM DG SOI MOSFET* is because of the screening of the drain potential by the induced step surface potential profile at the back gate.

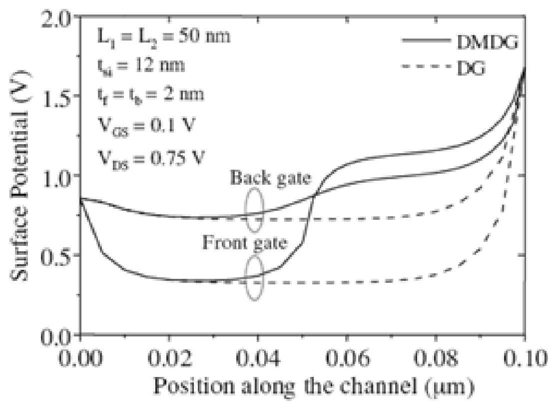

Fig 1.16 (a) Surface potential profiles at the front gate and the back gate for the DG and the DM DG-SOI MOSFETs with a channel length L = 0.1μm ($L_1 = L_2$ = 0.05 μm).

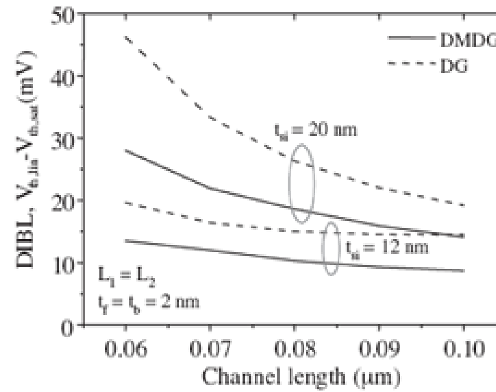

Fig. 1.16 (b) DIBL of the DG and the DMDG SOI MOSFETs for different channel lengths with $L_1 = L_2$

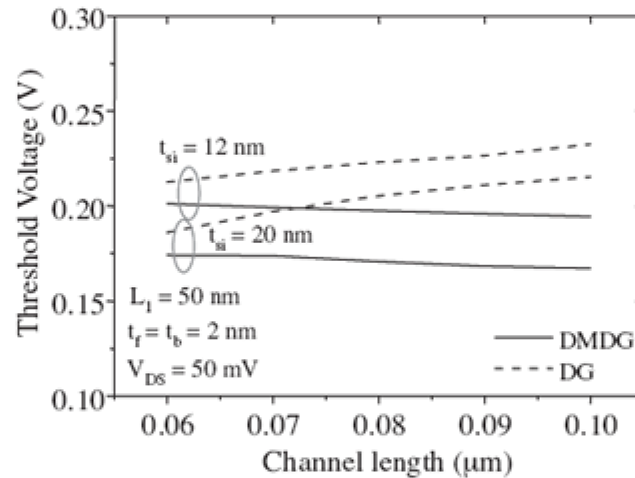

Fig. 1.16 (c) Threshold voltage of the DG and the DMDG SOI MOSFETs for different channel lengths (L_1 fixed at 0.05 μm).

Fig 1.16 Short channel effects in DM DG-SOI MOSFET due to induced Back-gate step potential.
Source: M. Jagadesh Kumar and G. Venkateshwar Reddy [66]

G. Venkateshwar Reddy et. al. [69] explored the novel features of an asymmetric double gate single halo *(DG-SH)* doped *SOI MOSFET* theoretically and compared with a conventional asymmetric *DG SOI MOSFET*. It has been observed that the application of single halo to the double gate structure resulted in threshold voltage roll-up, reduced *DIBL*, high drain output resistance, kink free output characteristics and increase in the breakdown voltage when compared with a conventional *DG* structure, as shown in figure 1.17

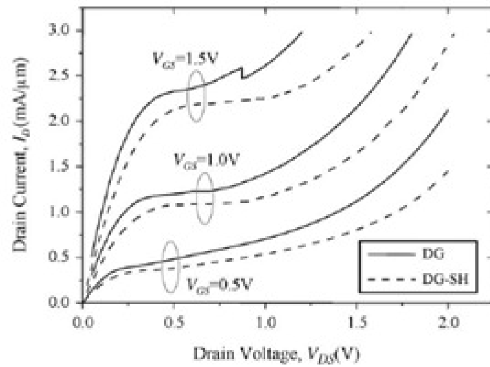

Fig. 1.17 (a) I_D -V_{DS} characteristics of the DG-SH and DG-SOI MOSFETs for a channel length L= 0.1 μm with a film thickness of 20 nm.

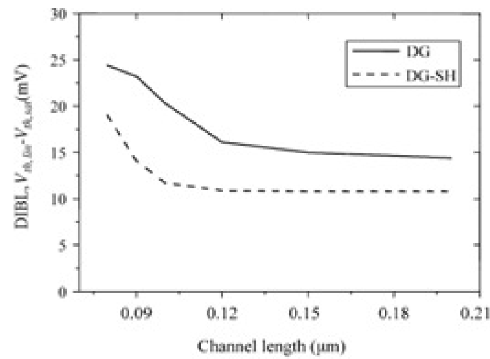

Fig. 1.17 (c) DIBL of DG-SH and DG SOI MOSFETs is plotted for different channel lengths for a film thickness of 20 nm.

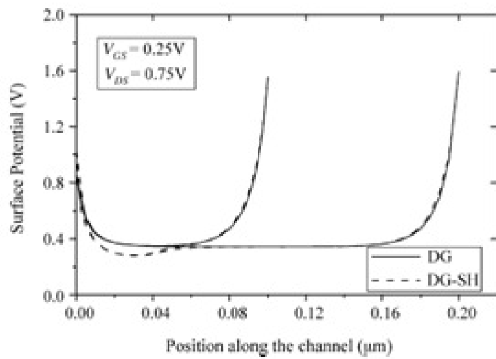

Fig. 1.17 (b) Surface potential profiles of DG-SH and DG-SOI MOSFETs for channel lengths 0.2 and 0.1 μm with a film thickness of 20 nm.

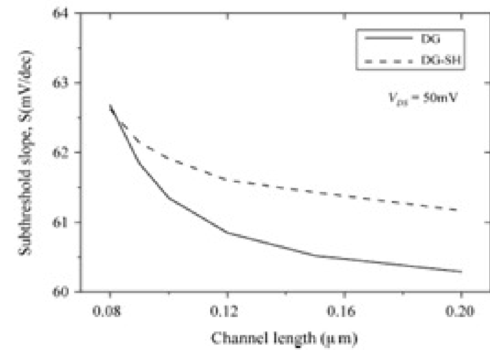

Fig. 1.17 (d) Subthreshold slope of DG-SH and DG SOI MOSFETs is plotted for different channel lengths for a film thickness of 20 nm.

Fig. 1.17 Performance characteristics of DG-SH and DG SOI MOSFET.
Source: G. Venkateshwar Reddy et. al. [69]

Wei Long, Haijiang Ou, Jen-Min Kuo, and Ken K. Chin [67] proposed **dual-material single-gate field effect transistor**. Where, the gate of the *DMGFET* consisted of two laterally contacting materials, as shown in figure 1.18, with different work functions. Wei Long et. al. observed:

- Due to this work function difference, the threshold voltage near the source is more positive than that near the drain (for n-channel *FET*, the opposite for p-channel *FET*), resulting in a more rapid acceleration of charge carriers in the channel and a screening effect to suppress short-channel effects.

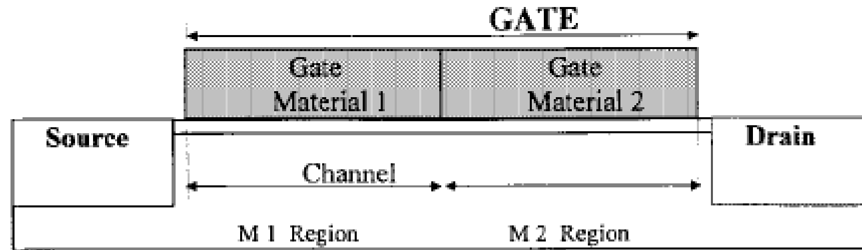

Fig. 1.18 Structure of DMG-FET. Source: Wei Long, Haijiang Ou, Jen-Min Kuo, and Ken K. Chin [67]

- The simulated longitudinal electric field distribution of the *DMG-HFET* has two peaks, as shown in Fig.1.19 (a). That of the conventional **single-material gate field effect transistor** is a single peak.
- By enhancing the electric field, and therefore the electron velocity, near the source, plays a predominant role in the overall carrier transport efficiency of the *FET* as shown in Fig. 1.19 (b).

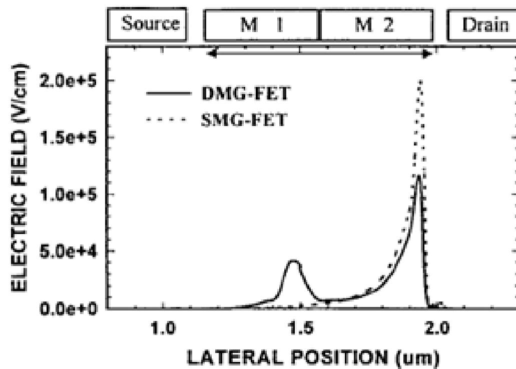

Fig. 1.19 (a) Simulated channel electric field distribution of DMGFET. The distribution of conventional SMGFET is also shown as a contrast (Vgs = -0.4; Vds = 1.4 V). Source: Wei Long et. al [67]

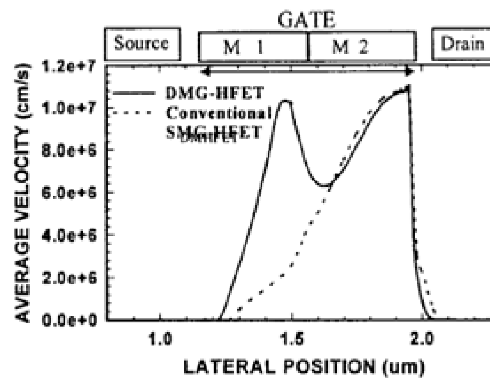

Fig. 1.19 (b) Simulated average electron velocity profile along the channel of DMG-FET is compared with that of the conventional SMG-FET. Bias is same as in previous figure. Source : Wei Long et. al [67]

- The *DMG* structure can suppress short-channel effects due to the screening effect, which is induced by a step change of the potential along the channel. Fig. 1.19 (c) shows the channel potential profiles for various drain biases. Beyond 0.5 V drain

voltage, i.e., after current saturation, the additional drain voltage increase is not absorbed under the M1 but under the M2.

- The threshold voltage of the *DMG-FET* is about the same as a conventional *SMG-FET* with the same gate material as M1 of the *DMG-FET* as shown in figure 1.19 (d). Therefore, the channel region under M2 has more freedom of optimization.

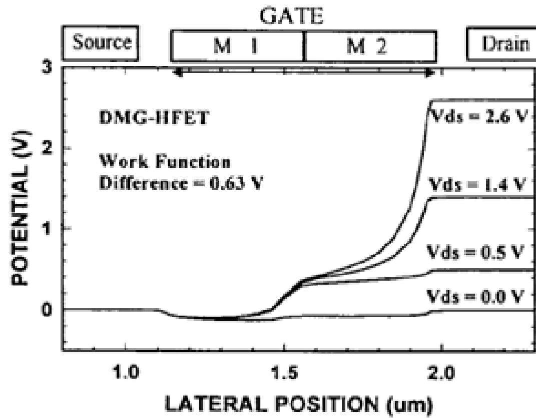

Fig 1.19 (c) Simulated channel potential profiles of DMG-FET for various drain biases. Screening effect is clearly seen. Source: Wei Long et. al [67]

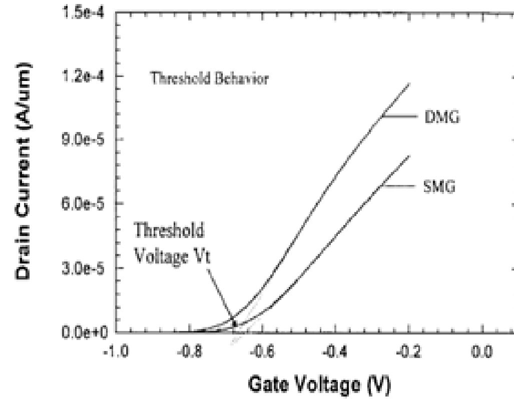

Fig. 1.19 (d) Threshold behaviors of dual material gate HFET (DMG-HFET) and conventional SMG-HFET. Very close values (-0.67 V for DMG and -0.65V for SMG) of threshold voltages have been extrapolated. Source: Wei Long et. al [67]

1.4 This Work

In this work, symmetric *DM DG FD SOI MOSFET* has been analyzed. The analytical model for the *MOSFET's* electrical parameters have been developed and compared with the results for the device parameters obtained by numerical analysis *(ATLAS)*. It has been shown that this structure provides for significantly improved electron transport efficiency and high frequency behavior of the device. Since for obtaining optimal device performance, ion implantation is invariably used for doping the body region, the impurity distribution in the body region is assumed to be non-uniform. Also because, the accurate device models are required for designing *VLSI* circuits, the impurity distribution in the body region has been assumed to be Pearson IV distribution (rather than ideal Gaussian distribution function) which matches the implanted distribution very closely. The noise analysis (in analysis of thermal and flicker noise) of the proposed device has also been carried out and it has been shown that the proposed structure offers improved noise

behavior. A neural network has also been developed which takes five major material /structural parameters of the *MOSFET* (namely silicon layer thickness (t_{si}), oxide layer thickness (t_{ox}), channel length ($L_g = L_1 + L_2$), drain-source voltage (V_{ds})and gate-source voltage (V_{gs})) as inputs and gives five major device parameters (surface potential (ϕ_s), electric field distribution (E_x), drain-source current (I_{ds}), transconductance (g_m) and cut-off frequency (f_c)) as outputs for a feasible *DM DG SOI MOSFET*. In case the input parameters do not relate to a feasible device the neural network does not converges.

This thesis is organized in five chapters. In Chapter-II, *2D* analytical model for potential distribution, electric field distribution, electron velocity distribution and subthreshold swing in *n*-channel *DM DG FD SOI MOSFET* is presented. In the analysis, the drain induced barrier lowering (*DIBL*) has been taken into account. A Pearson IV and ideal Gaussian distribution have been assumed in the body region and its consequences on the potential and electric field distribution have been compared. The same analysis is repeated using numerical analysis and the results obtained from both the proposed analytical model and the numerical analysis (using device simulator *ATLAS*) have been compared. In Chapter-III, the same has been done for the device parameter: threshold voltage (V_{th}), device capacitance (C_T), drain current characteristics (I_{ds}), transconductance (g_m), drain-resistance (r_{ds}), cut-off Frequency (f_c) and transit time (τ). The analysis of noise behavior of the proposed device has also been presented in this chapter. In Chapter-IV, a neural network which takes the device material/structural parameters as inputs and generates electrical parameters of the device as outputs has been described. The work is concluded in Chapter -V.

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Chapter-II

2-D ANALYTICAL MODEL FOR POTENTIAL AND ELECTRIC-FIELD DISTRIBUTION IN DM DG FD SOI MOSFET

2.1 Introduction

According to the Brew's scaling theory [70], the doping concentration in the body should be increased in the bulk *Si MOSFET* to alleviate the short-channel effects. Typically, the required doping concentration for a gate length less than $0.1\,\mu m$ is more than $10^{18}\ cm^{-3}$ [71]. Such high-doping concentration degrades device performance due to decreased mobility and increased junction capacitance. A *DG FD SOI-MOSFET* (see figure 2.1), was proposed to overcome the scaling limitations of bulk *Si MOSFETs*. In this structure two gates simultaneously control the carrier charge and current flow through the body region [72].

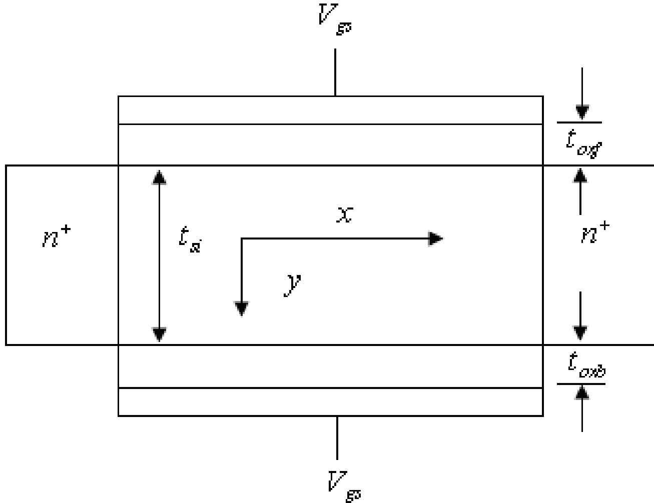

Fig 2.1 Cross-sectional view of a Double-Gate Fully-Depleted SOI MOSFET.

Excellent high speed and performance have been achieved in *DG FD SOI MOSFET* through improved design, use of high quality material and processing innovations [73]-[75]. It may be mentioned that in bulk *Si MOSFET,* the threshold voltage decreases as

the channel length shrinks, due to charge sharing between the source and drain. This problem is effectively solved in *DG FD SOI MOSFETs* due to a small channel depth [76].

The potential distribution in *DG FD SOI MOSFET* differs greatly from that in bulk *Si MOSFET* because in the former the device structure is symmetric and body doping concentration is low [77]. In double-gate *SOI MOSFETs*, the potential in the middle of the channel is more sensitive to the gate length than that at the surface [71]-[72]. The whole silicon film is into strong inversion in case of *DG FD SOI MOSFETs*. As the entire silicon layer is able to carry the current, the current capability of these devices is greater than that of bulk *Si MOSFETs*.

It has been demonstrated that the *DG FD SOI MOSFET* structure offers greatly reduced short channel effects but does not improve the electron transport efficiency [78]-[82]. Electron transport efficiency (assuming *n*-channel *MOSFET*) is related to the average electron transport velocity traveling through the channel which depends on the electric field distribution along the channel. In a *MOSFET*, in general, electrons enter into the channel initially with a low velocity and gradually get accelerated towards the drain. The electrons move fast in the region near drain but comparatively slow in the region near the source. Therefore, the performance of the device is affected by the relatively low electron drift velocity in the channel near the source.

In this work, a structure named as symmetric *DM DG FD SOI MOSFET* which offers improved electron transport efficiency, is proposed. The proposed structure, as shown in the figure 2.2, has two metals in the gate (both side) M1 and M2 with different work functions (*Appendix: A*). The work function of metal gate M1 is greater than the work function of metal gate M2 for *n*-channel *MOSFET* and vice-versa for a *p*-channel *MOSFET*. Due to this work function difference, the gate transport efficiency is improved by modifying the electric field distribution and surface potential profile. The step potential profile ensures reduction in *SCEs*. Also the peak electric field at the drain side is reduced, which ensures that the average electric field under the gate is increased leading to greater control of gate over the conductance of the channel which in turn leads to the increased electron transport efficiency. The overall device performance (particularly *RF* performance) greatly depends upon the doping distribution in the body region.

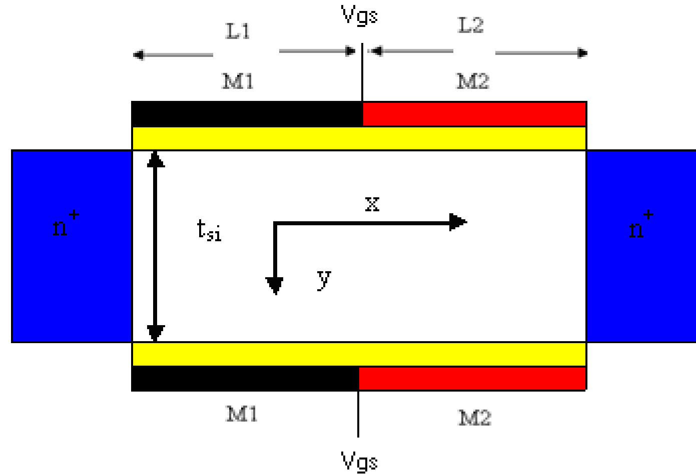

Fig 2.2 Cross-sectional view of a symmetric Dual-Material Double-Gate Fully-Depleted SOI MOSFET.

For the purpose of *IC* design the near exact device model is essential. Therefore, it is necessary to carry out the analysis for exact relationship between the device material and structure parameters with the electrical characteristics of the device. For this, the device behavior needs to be analyzed assuming a doping distribution as close to practically obtained doping distribution as possible [83]. For improved device performance, the body region is doped by ion implantation process. The next section discusses the ion implanted impurity distribution.

2.2 Ion Implantation in Thin Silicon Film

The introduction of ions into a substrate for changing its properties is called ion-implantation. During ion implantation, dopant atoms are vaporized, accelerated and directed at a silicon substrate.

The beam of ionized dopants enters the crystal lattice, collide with silicon atoms, and gradually lose energy, finally coming to rest at some depth within the lattice as shown in the figure 2.3. The average depth is controlled by adjusting the energy and dose of the dopant. For the dopant, ion energies varying from *1 keV* to *1 MeV*, the average penetration depth varies from *100 Å* to *10 µm*. The range of ion dose varies from 10^{12} $ions/cm^2$ for threshold adjustment to 10^{18} $ions/cm^2$ for buried insulators. Ion implantation is used to replace the chemical or doped oxide source wherever possible and is extensively used in device fabrication [84, 85].

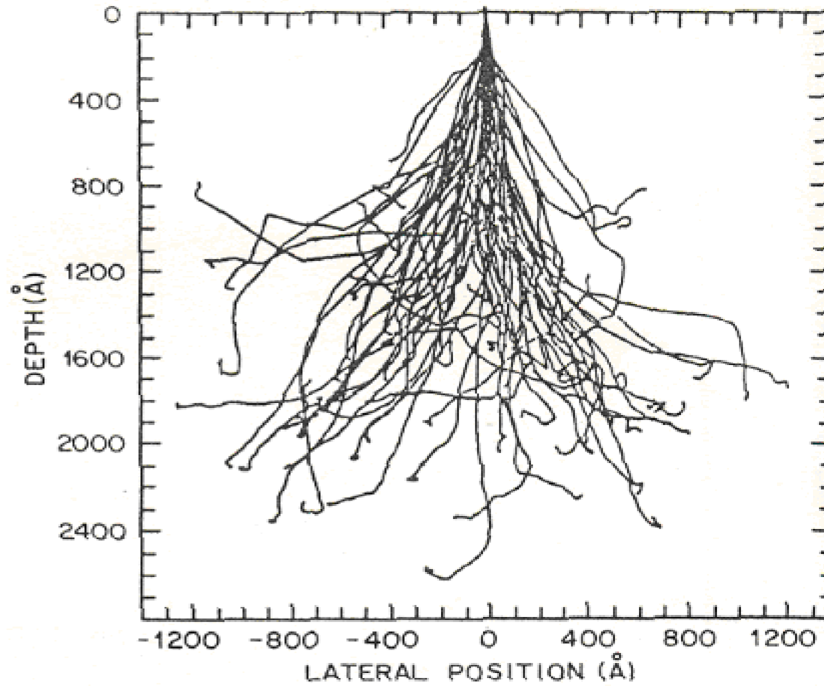

Fig 2.3 Monte Carlo calculation of 128 ion tracks for 50 keV Boron implanted into Silicon.

2.2.1 Doping Distributions

As discussed, the performance of the device depends greatly on impurity profile, in the body region. The implanted ion distribution in general is given by

$$N_a(y) = N_d \cdot f(y) \tag{2.01}$$

where, N_d is the total implant dose per unit area and $f(y)$ is the probability density function (*PDF*). The parameters associated with this *PDF*, $f(y)$, are given by

a) The projected range, $R_p = \int_{-\infty}^{+\infty} y \cdot f(y)\, dy$ (2.02)

b) The standard deviation, $\sigma = \left[\int_{-\infty}^{+\infty} (y - R_p)^2 \cdot f(y)\, dy \right]^{1/2}$ (2.03)

c) The skewness, $\gamma = \int_{-\infty}^{+\infty} \frac{(y - R_p)^3 \cdot f(y)}{\sigma^3}\, dy$ (2.04)

d) The kurtosis, $\beta = \int_{-\infty}^{+\infty} \frac{(y - R_p)^4 \cdot f(y)}{\sigma^4} dy$ (2.05)

These parameters are determined so as to fit an assumed function to an experimentally determine doping profiles [86]-[88], with the condition, $\int_{-\infty}^{+\infty} f(y)\,dy = 1$. The numerical values for these parameters are given in papers [89, 90] and fitted to a polynomial in paper [91] through

$R_p = \sum_{i=1}^{n} a_i \cdot E^i$ and $\sigma = \sum_{i=1}^{n} b_i \cdot E^i$ for n = 1,2,3,4……… Here, E is the implantation energy and a & b are the coefficients for silicon as target, given in tables 2.1 and 2.2 respectively.

Table 2.1 *Coefficients for R_p in Silicon*

Coefficients	Boron	Phosphorous	Antimony	Arsenic
a_1	3.338×10^{-3}	1.259×10^{-3}	8.887×10^{-4}	9.818×10^{-4}
a_2	-3.308×10^{-6}	-2.743×10^{-7}	-1.013×10^{-15}	-1.022×10^{-5}
a_3		1.290×10^{-9}	8.372×10^{-8}	9.067×10^{-8}
a_4			-3.056×10^{-10}	-3.442×10^{-10}
a_5			4.028×10^{-13}	4.608×10^{-13}

Table 2.2 *Coefficients for σ_p in Silicon*

Coefficients	Boron	Phosphorous	Antimony	Arsenic
b_1	1.781×10^{-3}	6.542×10^{-4}	2.674×10^{-4}	3.652×10^{-4}
b_2	-2.086×10^{-5}	-3.161×10^{-6}	-2.885×10^{-6}	-3.82×10^{-6}
b_3	1.403×10^{-7}	1.371×10^{-8}	2.311×10^{-8}	3.235×10^{-8}
b_4	-4.545×10^{-10}	-2.252×10^{-11}	-8.310×10^{-11}	-1.202×10^{-10}
b_5	5.525×10^{-13}		1.084×10^{-13}	1.601×10^{-13}

- Uniform Distribution

The Uniform distribution is a special case of equation (2.01) with $f(y) = 1$.

- Gaussian Distribution

This is the simplest approximation to an Ion-implanted Profile. This profile is characterized by the projected range (R_p), the average depth of the implanted ions and standard deviation (σ), the distribution of ions about that depth. The probability density function $f(y)$ for a Gaussian distribution is given as

$$f(y) = \frac{1}{\sigma.\sqrt{2.\pi}}.\exp\left(-\frac{(y-R_p)^2}{2.\sigma^2}\right) \tag{2.06}$$

Gaussian distributions have a skewness of "zero" and a kurtosis of "three". The approximation of implanted doping profile with a Gaussian distribution is only accurate up to first order. The Gaussian distribution with different (R_p) and different standard deviation (σ) is shown in figure 2.4 (a) and (b) respectively.

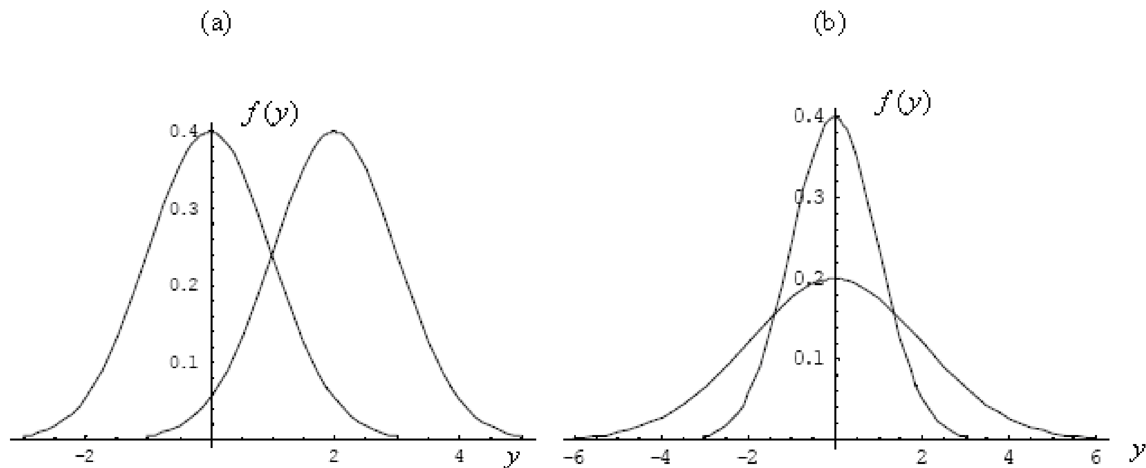

Fig 2.4 Gaussian distribution with different (a) means and (b) standard deviations.

- Pearson IV distribution

The implanted dopant profile is somewhat asymmetric due to bounce back of some ions, in contrast to Gaussian distribution which is symmetric. To characterize the actual implanted profile, it is required to consider the higher moments also i.e. skewness and kurtosis. Skewness measures the asymmetry of the distribution -

positive skewness places the peak of the distribution closer to the surface than (R_p) and the kurtosis measures how flat the top of a distribution is. These two higher moments are included in the Pearson IV distribution.

The Pearson distribution is given by the following differential equation:

$$\frac{dg(y)}{dy} = \frac{(y-a)g(y)}{b_o + b_1 \cdot y + b_2 \cdot y^2}; \tag{2.07}$$

where, $g(y)$ is the frequency function, constants a, b_o, b_1 and b_2 are obtained with the help of four moments [92-93].

$$a = -\frac{\gamma \cdot \sigma \cdot (\beta + 3)}{A}; \qquad b_o = -\frac{\sigma^2 (4 \cdot \beta - 3 \cdot \gamma^2)}{A}; \qquad b_1 = a;$$

$$b_2 = -\frac{(2 \cdot \beta - 3 \cdot \gamma^2 - 6)}{A}; \qquad A = 10 \cdot \beta - 12 \cdot \gamma^2 - 18;$$

Figure 2.5 shows the comparison of the Gaussian, Pearson and measured profiles [91].

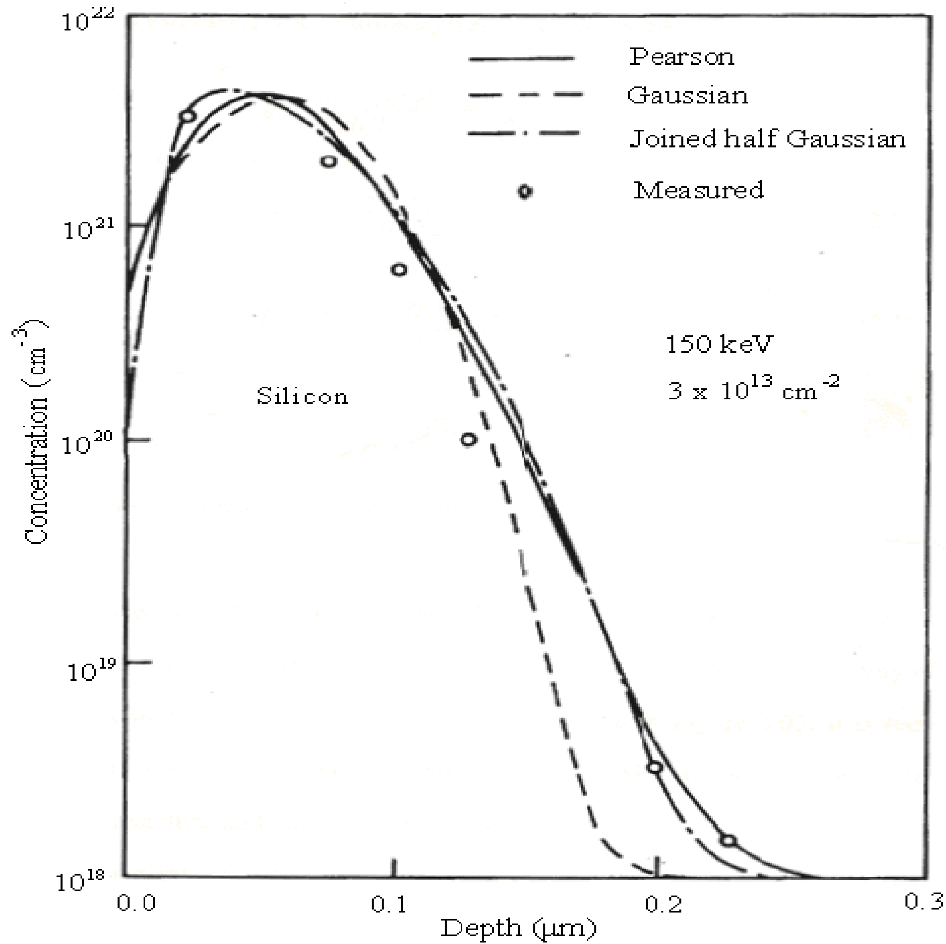

Fig 2.5 Comparison of implantation models (Gaussian and Pearson) and measured values.

The solutions of the above differential equation (2.07) are:

<u>Case -1</u> $b_1^2 - 4 \cdot b_o \cdot b_2 < 0$: (2.08)

$$\ln g(y) = \frac{1}{2 \cdot b_2} \cdot \ln\left|b_o + b_1 \cdot y + b_2 \cdot y^2\right| - \frac{b_1/b_2 + 2 \cdot a}{\left(4 \cdot b_2 \cdot b_o - b_1^2\right)^{1/2}} \arctan \frac{2 \cdot b_2 \cdot y + b_1}{\left(4 \cdot b_2 \cdot b_o - b_1^2\right)^{1/2}}$$

<u>Case- 2</u> $b_1^2 - 4 \cdot b_o \cdot b_2 > 0$: (2.09)

$$\ln g(y) = \frac{1}{2 \cdot b_2} \cdot \ln\left|b_o + b_1 \cdot y + b_2 \cdot y^2\right| - \frac{b_1/b_2 + 2 \cdot a}{\left(b_1^2 - 4 \cdot b_2 \cdot b_o\right)^{1/2}} \ln\left|\frac{2 \cdot b_2 \cdot y + b_1 - \left(b_1^2 - 4 \cdot b_o \cdot b_2\right)^{\frac{1}{2}}}{2 \cdot b_2 \cdot y + b_1 + \left(b_1^2 - 4 \cdot b_2 \cdot b_o\right)^{1/2}}\right|$$

<u>Case -3</u> $b_1^2 - 4 \cdot b_o \cdot b_2 = 0$: (2.10)

$$\ln g(y) = \frac{1}{2 \cdot b_2} \cdot \ln\left|b_o + b_1 \cdot y + b_2 \cdot y^2\right| - \frac{b_1/b_2 + 2 \cdot a}{2 \cdot b_2 \cdot y + b_1} \ ;$$

For the purpose of analysis in this work, the values of R_p, σ, γ and β have chosen and the values of the constants a, b_o, b_1 and b_2 were calculated. After calculating these values, above three cases were checked and found that $b_1^2 - 4 \cdot b_o \cdot b_2 > 0$. Therefore using equation (2.01) and (2.09), we get

$$\ln\left(\frac{N_a(y)}{N_d}\right) = \frac{1}{2 \cdot b_2} \cdot \ln\left|b_o + b_1 \cdot \left(y - R_p\right) + b_2 \cdot \left(y - R_p\right)^2\right| - \frac{b_1/b_2 + 2 \cdot a}{\left(b_1^2 - 4 \cdot b_2 \cdot b_o\right)^{1/2}} \ln\left(\left|\frac{2 \cdot b_2 \cdot \left(y - R_p\right) + b_1 - \left(b_1^2 - 4 \cdot b_o \cdot b_2\right)^{\frac{1}{2}}}{2 \cdot b_2 \cdot \left(y - R_p\right) + b_1 + \left(b_1^2 - 4 \cdot b_2 \cdot b_o\right)^{1/2}}\right|\right) = a_{111}$$

or

$N_a(y) = N_d \cdot \exp\left(a_{111}\right)$; where, $N_d = Q \cdot \int_{-\infty}^{+\infty} h(y)\, dy$; Q is implant dose and $h(y)$ is the normalized distribution function and satisfies $\int_{-\infty}^{+\infty} h(y)\, dy = 1$. Finally, the impurity ion distribution is given as

$$N_a(y) = N_d \cdot \exp\left(\begin{array}{l} \frac{1}{2 \cdot b_2} \cdot \ln\left| b_o + b_1 \cdot (y - R_p) + b_2 \cdot (y - R_p)^2 \right| - \\ \qquad \frac{b_1/b_2 + 2 \cdot a}{\left(b_1^2 - 4 \cdot b_2 \cdot b_o\right)^{\frac{1}{2}}} \ln\left(\left| \frac{2 \cdot b_2 \cdot (y - R_p) + b_1 - \left(b_1^2 - 4 \cdot b_o \cdot b_2\right)^{\frac{1}{2}}}{2 \cdot b_2 \cdot (y - R_p) + b_1 + \left(b_1^2 - 4 \cdot b_2 \cdot b_o\right)^{\frac{1}{2}}} \right| \right) \end{array} \right) \tag{2.11}$$

The calculated doping distribution for a set of R_p, σ, γ and β have calculated and plotted in figure 2.6 for Pearson IV distribution and figure 2.7 for a Gaussian distribution as can be seen Pearson IV distribution is much more asymmetric.

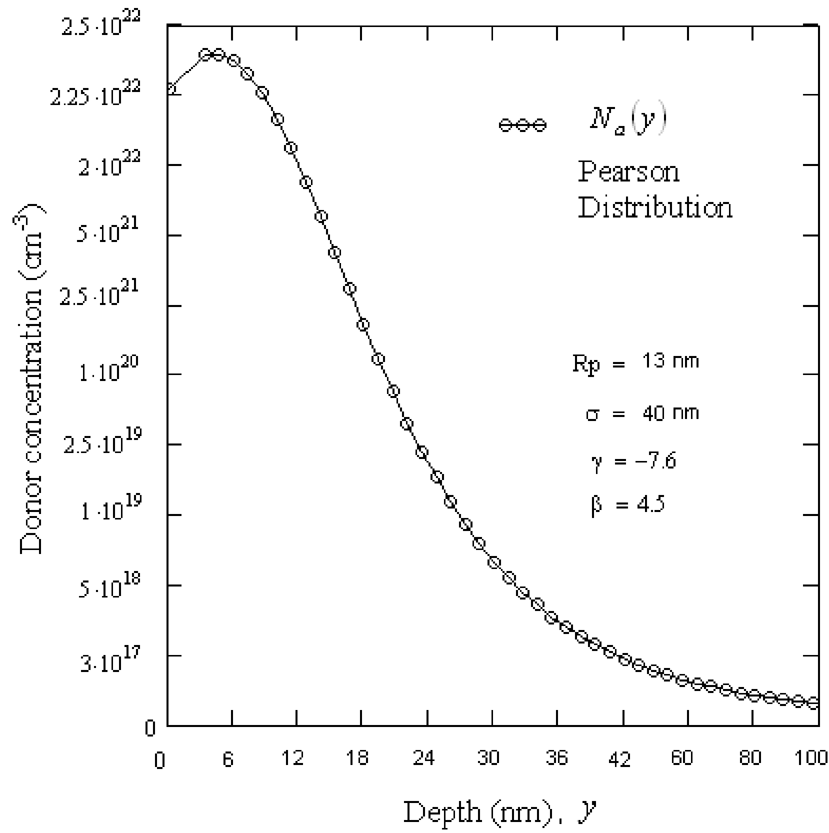

Fig 2.6 Doping concentration vs depth of the silicon using Pearson IV distribution.

2.3 Dual-Material Double-Gate FD SOI-MOSFET Operations

In dual-material double-gate *SOI MOSFET*, the front gate and the back gate consists of dual materials of different work functions as shown in figure 2.2. In general, the front gate bias voltages are chosen to be different to achieve optimal performance of the device.

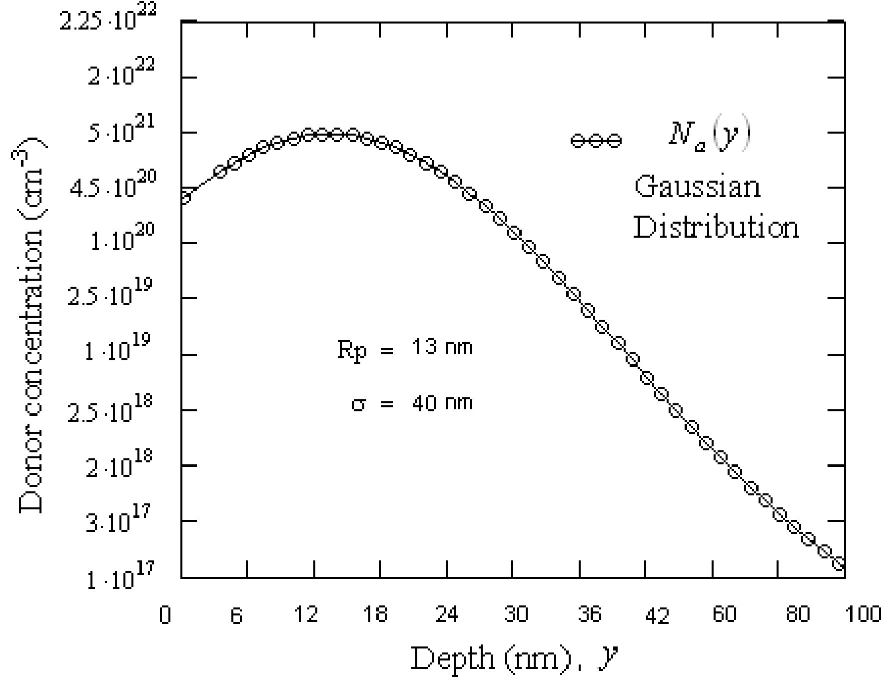

Fig 2.7 Doping concentration and depth of the silicon using Gaussian distribution

The relationship between the two gates voltages is: $V_{gs1} = K.V_{gs2}$, where the coefficient K accounts for the difference in the two gate in respect of the threshold voltages. In our calculation $K = 1$ is considered so that both the gates are at the same potential. The thickness of the *Si* layer has been assumed to be less than $x_{d\max}$, where $x_{d\max} = \sqrt{\frac{4.\varepsilon_{si}.\phi_F}{q.N_a(y)_{\max}}}$. Here $x_{d\max}$ is the maximum depletion width and $N_a(y)_{\max}$ is the maximum dopant concentration in *Si*. This ensures that the *Si* body is fully depleted.

2.4 Potential and Electric Field Distribution in Si

The potential distribution in the silicon layer before the onset of strong inversion is obtained by solving the Poisson's equation [72-73].

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{q \cdot N_a(y)}{\varepsilon_{si}}; \qquad \text{for} \quad 0 \le x \le L_g \quad \text{and} \quad 0 \le y \le t_{si} \qquad (2.12)$$

where, $N_a(y)$ is the Pearson IV doping distribution, dependent on the thickness of the

silicon layer, given by equation (2.11), q is the electron charge, ε_{si} is the permittivity of the silicon, L_g ($L_1 + L_2$) is the gate length and t_{si} is the silicon layer thickness.

The method for finding the analytical solution for $\phi(x, y)$ involves simplify the two-dimensional Poisson's equation into a one-dimensional equation with the help of appropriate boundary conditions. At low drain-source voltage the x-dependence of potential $\phi(x, y)$ for fully depleted *SOI MOSFET* can be approximated by a simple parabolic function [73].

$$\phi(x, y) = A_o(x) + A_1(x) \cdot y + A_2(x) \cdot y^2 \tag{2.13}$$

where, $A_o(x), A_1(x)$ and $A_2(x)$ are functions of x only. Equation (2.13) requires three conditions to have a non-trivial solution.

In Dual-Material Double-Gate structure, we have two different materials in both the gates (front as well as back) with work functions ϕ_{M1} and ϕ_{M2}, respectively. The potential distribution under gate M1, $\phi_1(x, y)$ and under gate M2, $\phi_2(x, y)$ respectively can be written as

$$\phi_1(x, y) = A_{1o}(x) + A_{11}(x) \cdot y + A_{12}(x) \cdot y^2; \quad \text{for} \quad 0 \le x \le L_1 \quad \text{and} \quad 0 \le y \le t_{si} \tag{2.14}$$

$$\phi_2(x, y) = A_{2o}(x) + A_{21}(x) \cdot y + A_{22}(x) \cdot y^2; \quad \text{for} \quad L_1 \le x \le L_1 + L_2 \quad \text{and} \quad 0 \le y \le t_{si} \tag{2.15}$$

where $A_{1o}(x), A_{11}(x)$, $A_{12}(x)$, $A_{2o}(x), A_{21}(x)$ and $A_{22}(x)$ are arbitrary coefficients. The Poisson's equation (2.12) is solved using the following boundary conditions:

i) $\phi_1(x,0) = \phi_{s1}(x)$, the surface potential under M1 (2.16a)

$\phi_2(x,0) = \phi_{s2}(x)$, the surface potential under M2 (2.16b)

ii) Electric flux at the front gate-oxide interface is

$$\left.\frac{\partial \phi_1(x, y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s1}(x) - V'_{gs1}}{t_{oxf}} \tag{2.17a}$$

$$\left.\frac{\partial \phi_2(x, y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s2}(x) - V'_{gs2}}{t_{oxf}} \tag{2.17b}$$

where ε_{ox} is the dielectric constant of the oxide-layer, t_{oxf} is oxide-layer

thickness at the front gate, $V'_{gs1} = V_{gs} - V_{fbf1}$ and $V'_{gs2} = V_{gs} - V_{fbf2}$ (2.18)

where V_{gs} is the gate-to-source bias voltage and V_{fbf1} & V_{fbf2} are the front-channel flat-band voltages of M1 & M2 respectively, given as.

$$V_{fbf1} = \phi_{M1} - \chi_{si} - \frac{E_g}{2 \cdot q} - V_T \ln\left(\left(\frac{N_a(y)}{n_i}\right)_{y=0}\right) \text{ and} \tag{2.19a}$$

$$V_{fbf2} = \phi_{M2} - \chi_{si} - \frac{E_g}{2 \cdot q} - V_T \ln\left(\left(\frac{N_a(y)}{n_i}\right)_{y=0}\right) \tag{2.19b}$$

where χ_{si} is the electron affinity of silicon, E_g is the silicon band gap at 300 K, given by

$$E_g = \left[1.16 - \left(\frac{7.02 \times 10^{-4} T^2}{1108 + T}\right)\right], \tag{2.20}$$

n_i is the intrinsic carrier concentration, given by

$$n_i = 3.1 \times 10^{16} T^{\frac{3}{2}} \exp\left(\frac{-E_g}{2kT}\right), \tag{2.21}$$

V_T is the thermal voltage, given by $V_T = \frac{kT}{q}$ and $N_a(y)$ is the Pearson IV doping distribution given by equation (2.11)

iii) Electric flux at the center plane of silicon layer:

$$\left.\frac{\partial \phi_1(x, y)}{\partial y}\right|_{y = \frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{V'_{gs1} - \phi_{B1}(x)}{t_{oxb}} = 0 \tag{2.22a}$$

$$\left.\frac{\partial \phi_2(x, y)}{\partial y}\right|_{y = \frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{V'_{gs2} - \phi_{B2}(x)}{t_{oxb}} = 0 \tag{2.22b}$$

where t_{oxb} is the back oxide-layer thickness and is same as that of t_{oxf}, $\phi_{B1}(x)$ and $\phi_{B2}(x)$ are the potential function along the back gate oxide-silicon interface under M1 and M2 respectively.

iv) Surface potential at the interface of two dissimilar gate material of the front gate is continuous

$$\phi_1(L_1,0) = \phi_2(L_1,0) \tag{2.23}$$

v) Electric flux at the interface of two material of the front gate is continuous

$$\left.\frac{\partial\phi_1(x,y)}{\partial x}\right|_{x=L_1} = \left.\frac{\partial\phi_2(x,y)}{\partial x}\right|_{x=L_1} \tag{2.24}$$

vi) The potential at the source end is

$$\phi_1(0,0) = \phi_{s1}(0) = V_{bi} \tag{2.25}$$

where $V_{bi} = \frac{E_g}{2} + V_T.\ln\left(\frac{N_a(y)}{n_i}\right)$ is the built-in potential across the body-source junction,

vii) The potential at the drain end is

$$\phi_2(L_1+L_2,0) = \phi_{s2}(L_1+L_2) = V_{bi} + V_{ds} \tag{2.26}$$

where V_{ds} is the applied drain-source bias.

The constants $A_{1o}(x)$, $A_{11}(x)$, $A_{12}(x)$, $A_{2o}(x)$, $A_{21}(x)$ and $A_{22}(x)$ in equations (2.14) & (2.15) can be found from the boundary conditions (i)-(iii). Using equation (2.16) in equations (2.14) & (2.15), we get

$$\phi_1(x,0) = A_{1o}(x) = \phi_{s1}(x) \quad \text{for } 0 \le x \le L_1 \ \ \&$$

$$\phi_2(x,0) = A_{2o}(x) = \phi_{s2}(x) \text{ for } L_1 \le x \le L_1 + L_2 \tag{2.27}$$

Substituting equation (2.27) into equations (2.14) & (2.15), we get

$$\phi_1(x,y) = \phi_{s1}(x) + A_{11}(x)\cdot y + A_{12}(x)\cdot y^2 \tag{2.28a}$$

$$\phi_2(x,y) = \phi_{s2}(x) + A_{21}(x)\cdot y + A_{22}(x)\cdot y^2 \tag{2.28b}$$

Differentiating equation (2.28) with respect to y, we get

$$\frac{\partial\phi_1(x,y)}{\partial y} = A_{11}(x) + 2.A_{12}(x).y \tag{2.29a}$$

$$\frac{\partial\phi_2(x,y)}{\partial y} = A_{21}(x) + 2.A_{22}(x).y \tag{2.29b}$$

Using equations (2.17) in equations (2.29), we get

$$\left.\frac{\partial \phi_1(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s1}(x) - V'_{gs1}}{t_{oxf}} = A_{11}(x)$$

or

$$A_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s1}(x) - V'_{gs1}}{t_{oxf}} \tag{2.30}$$

$$\left.\frac{\partial \phi_2(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s2}(x) - V'_{gs2}}{t_{oxf}} = A_{21}(x)$$

or

$$A_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s2}(x) - V'_{gs2}}{t_{oxf}} \tag{2.31}$$

Substituting equations (2.30) & (2.31) into equations (2.28), we get

$$\phi_1(x,y) = \phi_{s1}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s1}(x) - V'_{gs1}}{t_{oxf}} \cdot y + A_2(x) \cdot y^2 \tag{2.32a}$$

$$\phi_2(x,y) = \phi_{s2}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s2}(x) - V'_{gs2}}{t_{oxf}} \cdot y + A_2(x) \cdot y^2 \tag{2.32b}$$

Differentiating equations (2.32) with respect to y and using equations (2.22), we get

$$\left.\frac{\partial \phi_1(x,y)}{\partial y}\right|_{y=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s1}(x) - V'_{gs1}}{t_{oxf}} + 2.A_{12}(x).\frac{t_{si}}{2} = 0$$

or

$$A_{12}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s1}(x) - V'_{gs1}}{t_{oxf}.t_{si}} \tag{2.33}$$

and
$$\left.\frac{\partial \phi_2(x,y)}{\partial y}\right|_{y=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s2}(x) - V'_{gs2}}{t_{oxf}} + 2.A_{22}(x).\frac{t_{si}}{2} = 0$$

or $$A_{22}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s2}(x) - V'_{gs2}}{t_{oxf} .t_{si}} \tag{2.34}$$

Substituting equations (2.33) & (2.34) into equations (2.32), we get

$$\phi_1(x,y) = \phi_{s1}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s1}(x) - V'_{gs1}}{t_{oxf}} \cdot y - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s1}(x) - V'_{gs1}}{t_{oxf} .t_{si}} \cdot y^2 \tag{2.35a}$$

$$\phi_2(x,y) = \phi_{s2}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s2}(x) - V'_{gs2}}{t_{oxf}} \cdot y - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{\phi_{s2}(x) - V'_{gs2}}{t_{oxf} .t_{si}} \cdot y^2 \tag{2.35b}$$

Yan et al. [71] assumed that the punch-through current flows along the surface, which is not valid for a double-gate *SOI MOSFET* for the following reasons. The maximum potential at the *SOI MOSFET* center, ϕ_c, is more sensitive to gate length than potential at the surface, ϕ_s. Means that the punch-through current dominantly flows at the *SOI* center region. Since ϕ_c should be relevant to the punch-through current, we obtained the relation between ϕ_s and ϕ_c from equation (2.35) (i.e. $\phi_1(x,y) = \phi_{c1}(x)$ and $\phi_2(x,y) = \phi_{c2}(x)$ at $y = \frac{t_{si}}{2}$).

$$\phi_{s1}(x) = \frac{1}{1 + \frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{oxf}}} \left(\phi_{c1}(x) + \frac{\varepsilon_{ox}.t_{si}.V'_{gs11}}{4.\varepsilon_{si}.t_{oxf}} \right) \tag{2.36}$$

where $$V'_{gs11} = V_{gs} - V_{fbf1} = V_{gs} - \phi_{M1} + \chi_{si} + \frac{E_g}{2 \cdot q} + V_T \ln\left(\left(\frac{N_a(y)}{n_i} \right)_{y=\frac{t_{si}}{2}} \right) \tag{2.37}$$

and $$\phi_{s2}(x) = \frac{1}{1 + \frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{oxf}}} \left(\phi_{c2}(x) + \frac{\varepsilon_{ox}.t_{si}.V'_{gs22}}{4.\varepsilon_{si}.t_{oxf}} \right) \tag{2.38}$$

where $$V'_{gs22} = V_{gs} - V_{fbf2} = V_{gs} - \phi_{M2} + \chi_{si} + \frac{E_g}{2 \cdot q} + V_T \ln\left(\left(\frac{N_a(y)}{n_i} \right)_{y=\frac{t_{si}}{2}} \right) \tag{2.39}$$

Substituting equations (2.36) & (2.38) into equation (2.35), we get

$$\phi_1(x,y) = \left(1+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{t_{oxf}}\cdot y-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{t_{oxf}.t_{si}}\cdot y^2\right)\left(\frac{1}{1+\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{oxf}}}\left(\phi_{c1}(x)+\frac{\varepsilon_{ox}.t_{si}.V'_{gs11}}{4.\varepsilon_{si}.t_{oxf}}\right)\right)$$

$$-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{V'_{gs1}}{t_{oxf}}\cdot y+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{V'_{gs1}}{t_{oxf}.t_{si}}\cdot y^2 \tag{2.40}$$

and

$$\phi_2(x,y) = \left(1+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{t_{oxf}}\cdot y-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{t_{oxf}.t_{si}}\cdot y^2\right)\left(\frac{1}{1+\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{oxf}}}\left(\phi_{c2}(x)+\frac{\varepsilon_{ox}.t_{si}.V'_{gs22}}{4.\varepsilon_{si}.t_{oxf}}\right)\right)$$

$$-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{V'_{gs2}}{t_{oxf}}\cdot y+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{V'_{gs2}}{t_{oxf}.t_{si}}\cdot y^2 \tag{2.41}$$

The *2D* Poisson's equation has been simplified into two one-dimensional equation in terms of $\phi_{c1}(x)$ & $\phi_{c2}(x)$. The derivation involved is given in *Appendix: B*. The one-dimensional Poisson's equations are given as below.

$$\left(\frac{d^2\phi_{c1}(x)}{dx^2}\right)-\frac{1}{\lambda_1^2}\left(\phi_{c1}(x)-\left((1+A_1)V'_{gs1}-A_1.V'_{gs11}\right)\right) = \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}} \tag{2.42}$$

and

$$\left(\frac{d^2\phi_{c2}(x)}{dx^2}\right)-\frac{1}{\lambda_1^2}\left(\phi_{c2}(x)-\left((1+A_1)V'_{gs2}-A_1.V'_{gs22}\right)\right) = \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}} \tag{2.43}$$

where $N_a\left(\frac{t_{si}}{2}\right)$ is obtained from equation (2.11) thereby calculating potential at the

center of silicon layer. λ_1 (please see in *Appendix: B)* is the natural length designed to fulfill the condition:

$$\alpha = \frac{L_g}{2.\lambda_1}; \tag{2.44}$$

here, α is the scaling factor and L_g is the gate length. The relationship between oxide layer thickness, t_{ox} and silicon layer thickness, t_{si} can be obtained by substituting equation (2.44) into equation (b1.20) (please see in *Appendix: B).*

$$t_{ox} = \frac{\varepsilon_{ox}.L_g^2}{2.\alpha^2.\varepsilon_{si}.t_{si}} - \frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}} \tag{2.45}$$

For $\alpha = 2.8$, the relationship between t_{ox} and t_{si} for different gate lengths are plotted in figure 2.8 . For a particular gate length L_g, any point below the curve, representing a pair of values of t_{ox} and t_{si}, can be chosen.

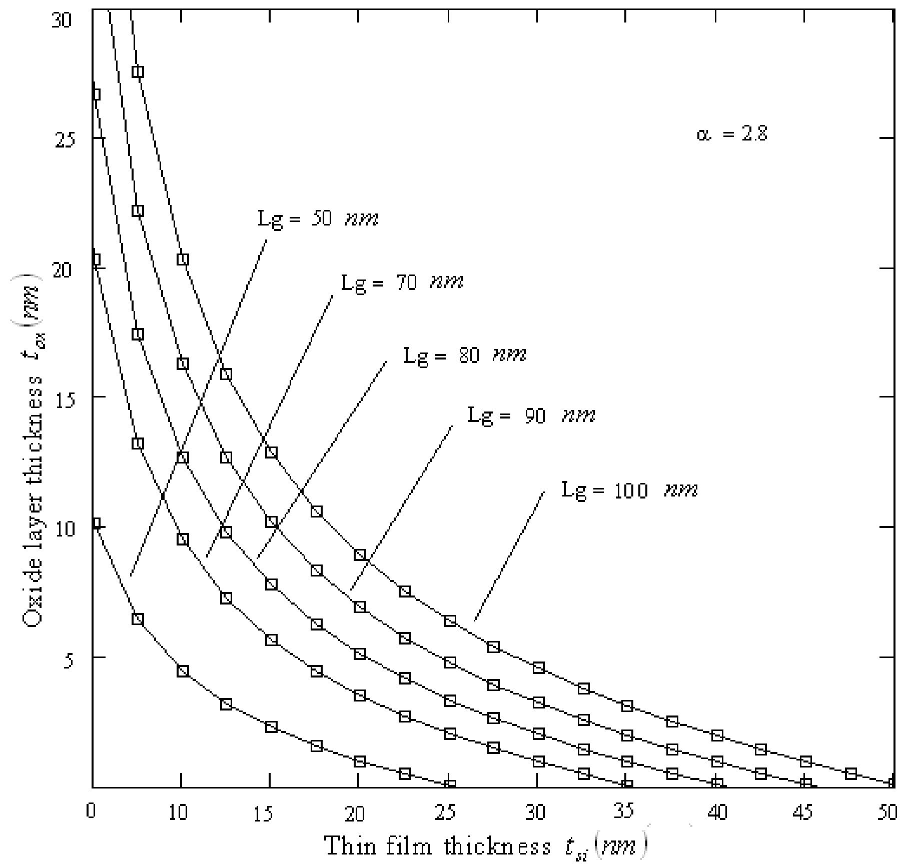

Fig 2.8 Relationship between oxide layer thickness, t_{ox} and silicon layer thickness, t_{si} for different values of gate length.

2.4.1 Potential Distribution

Potential distribution is an important parameter in device modeling, [71] as many other parameters are determined from it i.e. threshold voltage, channel field etc.

Assuming,

$$\phi_{f1}(x) = \phi_{c1}(x) - \left((1+A_1)V'_{gs1} - A_1.V'_{gs11}\right) + \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\ 2} \tag{2.46}$$

and

$$\phi_{f2}(x) = \phi_{c2}(x) - \left((1+A_1)V'_{gs2} - A_1.V'_{gs22}\right) + \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\ 2} \tag{2.47}$$

Differentiating equation (2.66) & (2.67) twice with respect to x, we get

$$\frac{d\phi_{f1}(x)}{dx} = \frac{d\phi_{c1}(x)}{dx}; \tag{2.48}$$

$$\frac{d^2\phi_{f1}(x)}{dx^2} = \frac{d^2\phi_{c1}(x)}{dx^2}; \tag{2.49}$$

and

$$\frac{d\phi_{f2}(x)}{dx} = \frac{d\phi_{c2}(x)}{dx}; \tag{2.50}$$

$$\frac{d^2\phi_{f2}(x)}{dx^2} = \frac{d^2\phi_{c2}(x)}{dx^2} \tag{2.51}$$

Substituting equations (2.46), (2.47), (2.49) and (2.51) into equations (2.42) & (2.43), we get

$$\frac{d^2\phi_{f1}(x)}{dx^2} - \frac{1}{\lambda_1^2}\left(\phi_{f1}(x) - \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\ 2}\right) = \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}$$

or

$$\frac{d^2\phi_{f1}(x)}{dx^2} - \frac{\phi_{f1}(x)}{\lambda_1^2} = 0; \tag{2.52}$$

Similarly,
$$\frac{d^2\phi_{f2}(x)}{dx^2} - \frac{1}{\lambda_1^2}\left(\phi_{f2}(x) - \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\ 2}\right) = \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}$$

or
$$\frac{d^2\phi_{f2}(x)}{dx^2} - \frac{\phi_{f2}(x)}{\lambda_1^2} = 0; \tag{2.53}$$

Equations (2.52) & (2.53) have a non-trivial solution, which is assumed to be

$$\phi_{f1}(x) = A_{011}.\exp\left(\frac{x}{\lambda_1}\right) + B_{011}.\exp\left(\frac{-x}{\lambda_1}\right); \tag{2.54}$$

$$\phi_{f2}(x) = A_{022}.\exp\left(\frac{(x-L_1)}{\lambda_1}\right) + B_{022}.\exp\left(\frac{-(x-L_1)}{\lambda_1}\right); \tag{2.55}$$

here A_{011}, A_{022}, B_{011} and B_{022} are arbitrary constants.

2.4.1.1 Potential at the Center of the Silicon Layer

The potential at the centre of the film is obtained by substituting the value of $\phi_{f1}(x)$ & $\phi_{f2}(x)$ from equations (2.54) & (2.55) into equations (2.46) & (2.47)

$$\phi_{c1}(x) = \left((1+A_1)V'_{gs1} - A_1.V'_{gs11}\right) - \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\ 2} + A_{011}.\exp\left(\frac{x}{\lambda_1}\right) + B_{011}.\exp\left(\frac{-x}{\lambda_1}\right)$$
$$\text{for} \quad 0 \le x \le L_1 \quad \text{and} \quad 0 \le y \le t_{si} \tag{2.56}$$

$$\phi_{c2}(x) = \left((1+A_1)V'_{gs2} - A_1.V'_{gs22}\right) - \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\ 2} + A_{022}.\exp\left(\frac{(x-L_1)}{\lambda_1}\right) + B_{022}.\exp\left(\frac{-(x-L_1)}{\lambda_1}\right)$$
$$\text{for} \quad L_1 \le x \le L_1 + L_2 \quad \text{and} \quad 0 \le y \le t_{si} \tag{2.57}$$

2.4.1.2 Surface Potential

Similarly, the surface potential is obtained by substituting the value of $\phi_{c1}(x)$ & $\phi_{c2}(x)$ from equations (2.56) & (2.57) into equations (2.36) & (2.38).

$$\phi_{s1}(x)=\frac{1}{1+\dfrac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{oxf}}}\left(\begin{array}{r}\left((1+A_1)V'_{gs1}-A_1.V'_{gs11}\right)-\dfrac{q.N_a\left(\dfrac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\,2}+\\ A_{011}.\exp\left(\dfrac{x}{\lambda_1}\right)+B_{011}.\exp\left(\dfrac{-x}{\lambda_1}\right)+\dfrac{\varepsilon_{ox}.t_{si}.V'_{gs11}}{4.\varepsilon_{si}.t_{oxf}}\end{array}\right)$$

or

$$\phi_{s1}(x)=\frac{1}{1+A_1}\left(\left((1+A_1)V'_{gs1}\right)-\frac{q.N_a\left(\dfrac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\,2}+A_{011}.\exp\left(\frac{x}{\lambda_1}\right)+B_{011}.\exp\left(\frac{-x}{\lambda_1}\right)\right)$$

$$\text{for} \quad 0\le x\le L_1 \quad \text{and} \quad 0\le y\le t_{si} \tag{2.58}$$

$$\phi_{s2}(x)=\frac{1}{1+\dfrac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{oxf}}}\left(\begin{array}{r}\left((1+A_1)V'_{gs2}-A_1.V'_{gs22}\right)-\dfrac{q.N_a\left(\dfrac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\,2}+\\ A_{022}.\exp\left(\dfrac{(x-L_1)}{\lambda_1}\right)+B_{022}.\exp\left(\dfrac{-(x-L_1)}{\lambda_1}\right)+\dfrac{\varepsilon_{ox}.t_{si}.V'_{gs22}}{4.\varepsilon_{si}.t_{oxf}}\end{array}\right)$$

or

$$\phi_{s2}(x)=\frac{1}{1+A_1}\left(\left((1+A_1)V'_{gs2}\right)-\frac{q.N_a\left(\dfrac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\,2}+A_{022}.\exp\left(\frac{(x-L_1)}{\lambda_1}\right)+B_{022}.\exp\left(\frac{-(x-L_1)}{\lambda_1}\right)\right)$$

$$\text{for} \quad L_1\le x\le L_1+L_2 \quad \text{and} \quad 0\le y\le t_{si} \tag{2.59}$$

here $A_{011}, A_{022}, B_{011}$ and B_{022} are determined using the boundary conditions from equations (2.23)-(2.26), [Equations for $A_{011}, A_{022}, B_{011}$ and B_{022} have been derived in *Appendix: C*] and the same are given below:

$$A_{011} = -\frac{1}{2}\frac{2.S.\exp\left(-\frac{L_1}{\lambda_1}\right) - 2.T_o.\exp\left(\frac{L_2}{\lambda_1}\right) - R - \exp\left(\frac{2L_2}{\lambda_1}\right).R}{\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - \exp\left(-\frac{L_1}{\lambda_1}\right)} \tag{2.60}$$

and

$$B_{011} = \frac{2.S.\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - 2.T_o.\exp\left(\frac{L_2}{\lambda_1}\right) - R - \exp\left(\frac{2L_2}{\lambda_1}\right).R}{2.\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - 2.\exp\left(-\frac{L_1}{\lambda_1}\right)} \tag{2.61}$$

$$A_{022} = -\frac{1}{2}\frac{\begin{pmatrix} -2.S + 2.\exp\left(\frac{L_1+L_2}{\lambda_1}\right).T_o + \exp\left(\frac{L_1}{\lambda_1}\right).R - R.\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) + 2.\exp\left(\frac{2L_2}{\lambda_1}\right).S + \\ \exp\left(-\frac{L_1}{\lambda_1}\right).R - \exp\left(-\frac{(L_1-2L_2)}{\lambda_1}\right).R - 2.T_o\exp\left(\frac{L_1+3L_2}{\lambda_1}\right) \end{pmatrix}}{\left(\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - \exp\left(-\frac{L_1}{\lambda_1}\right)\right)\left(-1+\exp\left(\frac{2L_2}{\lambda_1}\right)\right)} \tag{2.62}$$

$$B_{022} = -\frac{1}{2}\frac{\begin{pmatrix} -2.T_0.\exp\left(-\frac{L_1}{\lambda_1}\right) + 2.T_o.\exp\left(-\frac{(L_1-2L_2)}{\lambda_1}\right) + 2.\exp\left(\frac{(L_2)}{\lambda_1}\right).S - \\ \exp\left(\frac{L_1+L_2}{\lambda_1}\right).R + \exp\left(\frac{L_1+3L_2}{\lambda_1}\right).R - 2.\exp\left(\frac{3L_2}{\lambda_1}\right).S - \\ \exp\left(\frac{L_2-L_1}{\lambda_1}\right).R + \exp\left(\frac{-L_1+3L_2}{\lambda_1}\right).R \end{pmatrix}.\exp\left(\frac{L_2}{\lambda_1}\right)}{\left(\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - \exp\left(-\frac{L_1}{\lambda_1}\right)\right)\left(-1+\exp\left(\frac{2L_2}{\lambda_1}\right)\right)} \tag{2.63}$$

where $$R = -(\gamma_1 - \gamma_2); \tag{2.64}$$

$$S = V_{bi}(1 + A_1) - \gamma_1; \tag{2.65}$$

$$T_o = (V_{bi} + V_{ds}).(1 + A_1) - \gamma_2 \tag{2.66}$$

From equations (2.56), (2.57), (2.58) & (2.59), ϕ_s and ϕ_c can be determined. In figure 2.9, ϕ_s and ϕ_c for both *DM DG* and *SM DG SOI MOSFET* is plotted. For *SM DG SOI MOSFET*, the metal work function is assumed to be $\phi_M = 5V$.

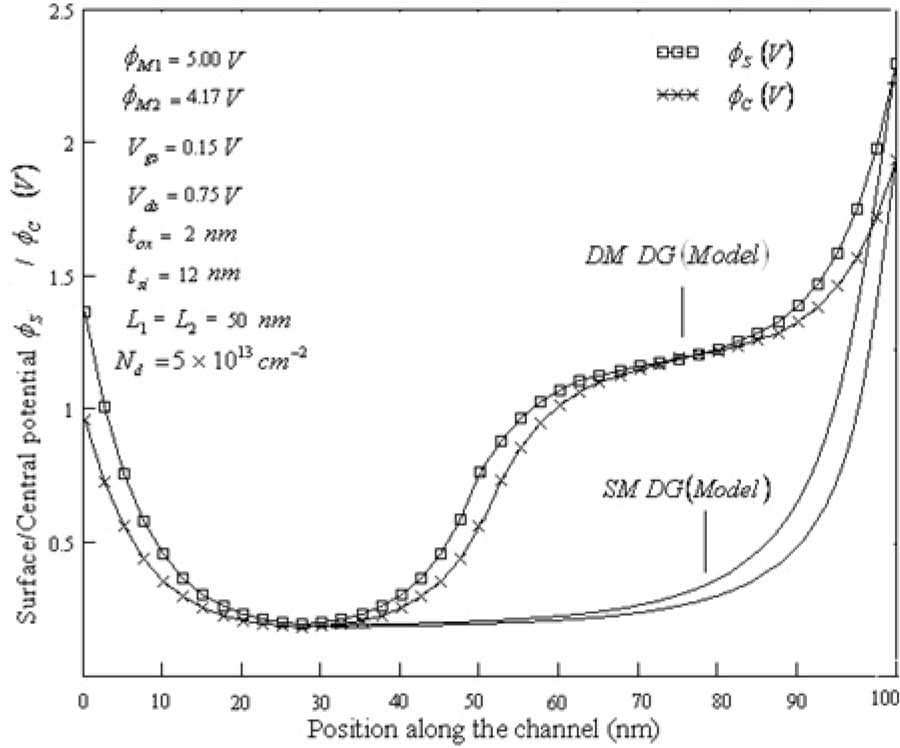

Fig 2.9 Potential profile at the surface and center of DM DG and SM DG FD SOI MOSFET (Model) for a channel length L_g = 100nm.

It is evident that the absolute value of ϕ_c is smaller than the ϕ_s [72]. It is also observed that the potential at the surface and center exhibits a step function in the surface. Due to this step function, the area under M1 of front gate of the *DM DG* structure is screened from the drain potential variations or we can say the step function suppresses the effect of the electric field induced by the drain-source potential in the region under M1. This means that the drain potential has very little effect on the drain current after saturation increasing the drain resistance. Figure 2.10 shows the comparison between the values calculated using analytical model and the corresponding values obtained using numerical solution (using *ATLAS*) for *DM DG* structure. As is evident from the figure 2.10, the calculated results using the analytical model are in excellent agreement with the simulation results (obtained using *ATLAS*).

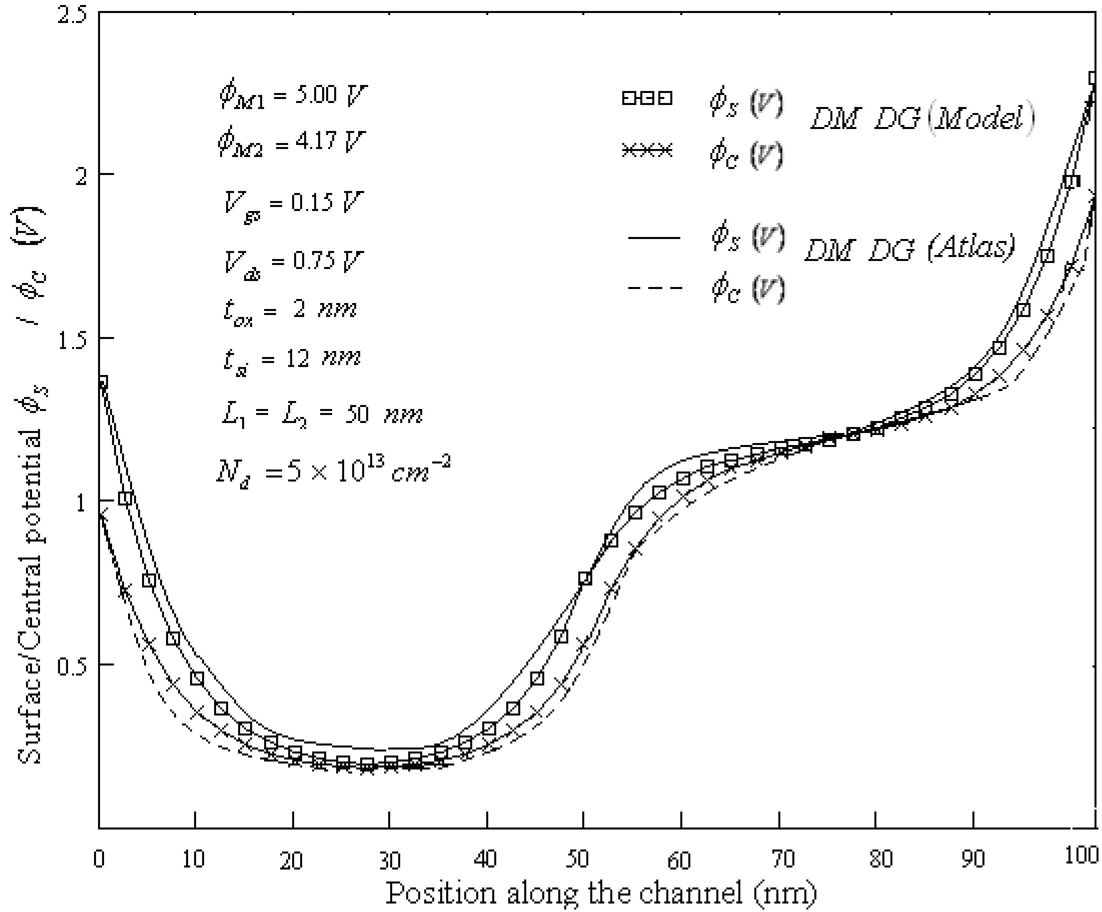

Fig 2.10 Comparison of analytical model and simulated values of potential at the surface and center of DM DG FD SOI MOSFET for a channel length L_g = 100nm.

Figure 2.11 shows the surface potential variation along the channel for $t_{si} = 6\,nm$ keeping other parameters as such. It is observed that the difference between the surface and center potential decreases as we decrease the film thickness, because for small silicon layer thickness, the center potential approaches towards surface potential. This means there is no significant difference between the two potentials when the film thickness is very small. Step function of potential becomes more flat as we decrease the silicon layer thickness as shown in figure 2.12. This is due to one-dimensional nature of electric field over major part of the device.

Figure 2.13 shows the variation of surface potential in *DM DG FD SOI MOSFET* for long channel length $L_g = 1000\,nm$. It is observed that the constant potential contour in a long channel device is mostly parallel to the Si/SiO_2 interface thereby making electric field one dimensional over most part of the device.

The surface potential as calculated using the analytical model and as obtained using device simulator *ATLAS* is also compared inn figure 2.13. As can be seen, the two results in excellent agreement.

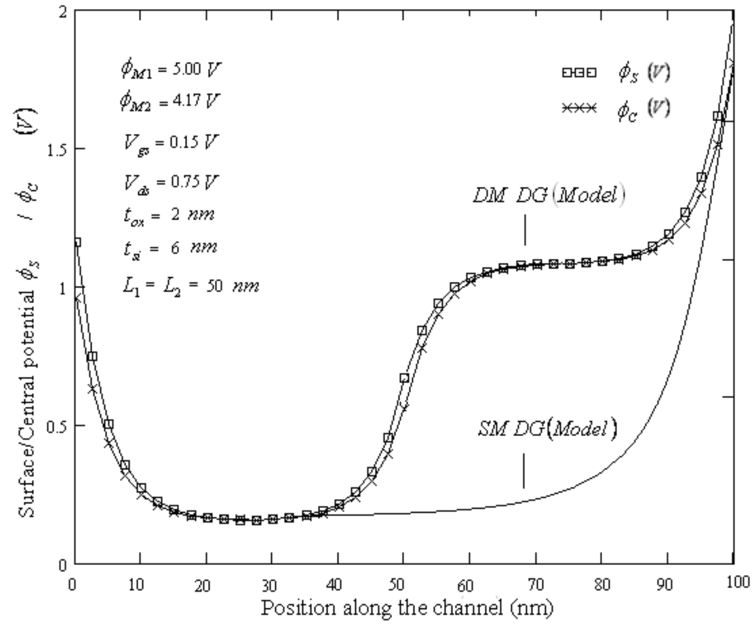

Fig 2.11 Potential profile at the surface and center of DM DG and SM DG FD SOI MOSFET (Model) for a channel length L_g = 100nm and t_{si} = 6nm.

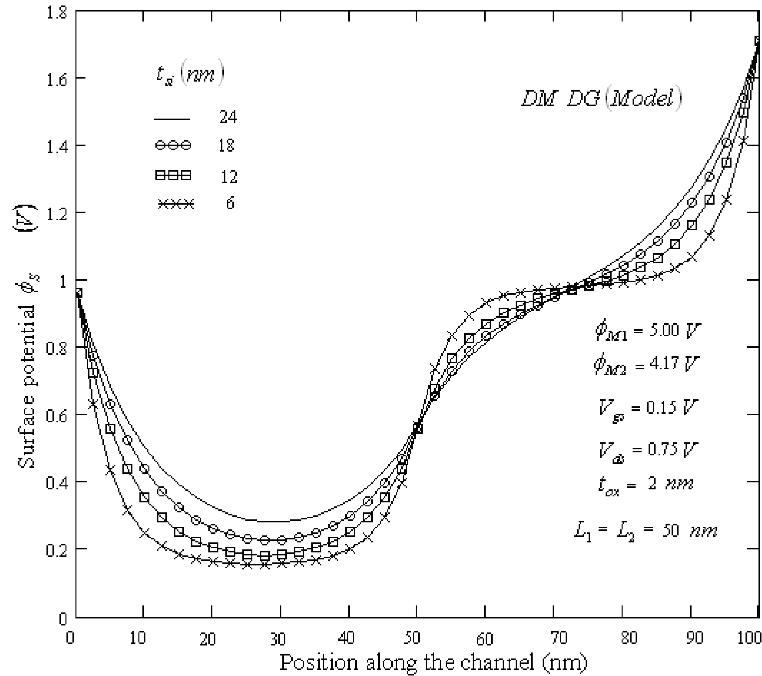

Fig 2.12 Potential profile at the surface of DM DG FD SOI MOSFET (Model) for a channel length L_g = 100nm for different values of film thickness.

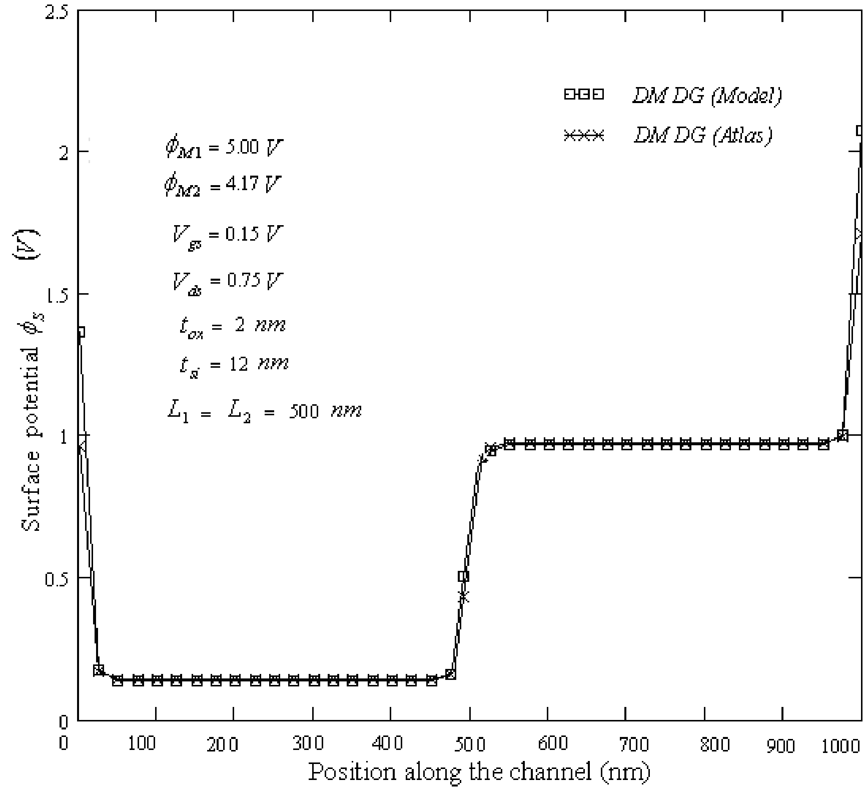

Fig 2.13 Potential profile at the surface of DM DG FD SOI MOSFET (Model) for a channel length L_g = 1000nm.

On comparing figure 2.13 and figure 2.12, where $L_g = 100\,nm$, it is seen that the constant potential contour becomes more curvilinear as the gate length decreases. This curvilinear nature of potential is due to the two-dimensional nature of the electric field in the channel.

Figure 2.14 shows the variation of the surface potential along the channel length for different values of oxide thickness for *DM DG* structure. On increasing the value of oxide thickness t_{ox} at the front end as well as at the back end, M1 and M2 lose their control over the channel thereby increasing the *DIBL*. However, continuous decrease in the oxide thickness definitely reduces the *DIBL,* but at the same time we have to account the tunneling across the thin oxide and hot-carrier effects.

Figure 2.15 shows the variation of surface potential along the channel, where L_1 is not equal to L_2, for different values of V_{ds}. For *DM DG SOI MOSFET,* the position of the minimum surface potential lies only under the M1 region of the gate due to the step function profile of surface potential. Also there is not much change in the minimum

surface potential for higher values of V_{ds}. Hence, the area under M1 is screened from the changes in the V_{ds}. However, there is enhancement in the values of surface potential near drain for increasing values of V_{ds} as shown in the figure 2.15.

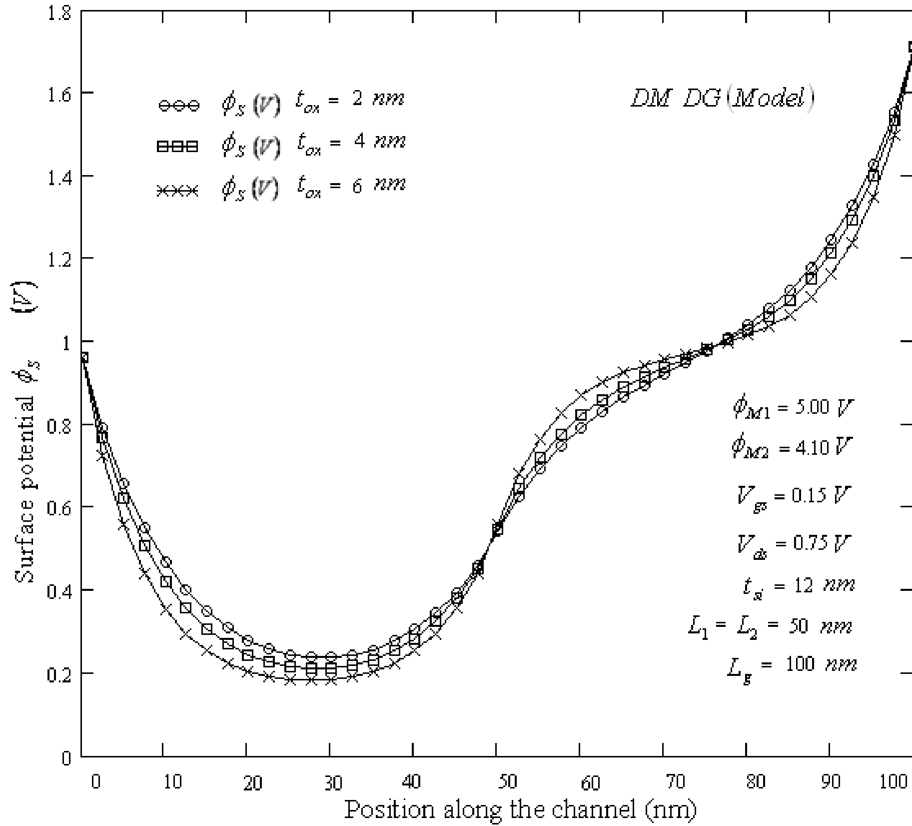

Fig 2.14 Potential profile at the surface of DM DG FD SOI MOSFET (Model) for a channel length L_g= 100nm for different values of oxide thickness.

Figure 2.16 shows the variation of the surface potential along the channel length for different values of V_{gs}. It is seen that the surface potential increases with increasing values of V_{gs} as expected.

Figure 2.17 shows the variation of the surface potential along the channel length for different combination of L_1 and L_2 keeping L_1+L_2 equal to 100 *nm*. It is observed that the position of minimum surface potential under M1 is shifting towards source as the length of M1 is reduced. Due to this the peak electric field in the channel shifts more towards the source end which makes the electric field distribution more uniform in the channel.

Figure 2.18 shows the variation of surface potential along the channel for uniform, Gaussian and Pearson IV doping distributions. It is observed that the potential in the channel is increased for the Pearson IV doping distribution as compared to the other two.

As the doping concentration increases depletion width decreases and the characteristics length, λ decreases which improves the Lg/ λ ratio leading to better short channel immunity. Closer look of the potential is also shown in the inset to proper differentiate the three doping distributions.

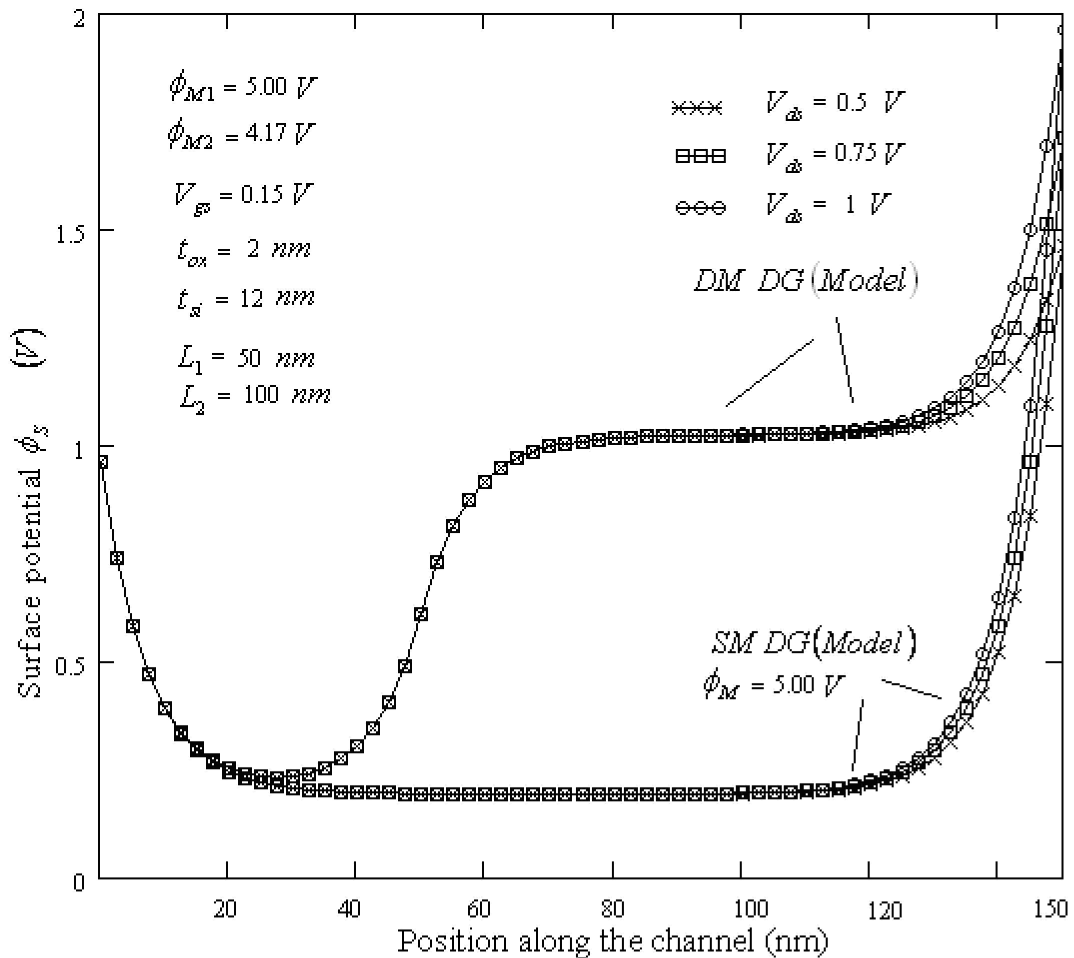

Fig 2.15 Potential profile at the surface of DM DG FD SOI MOSFET (Model) for a channel length L_g = 150nm where $L_1 \neq L_2$, for different values of V_{ds}.

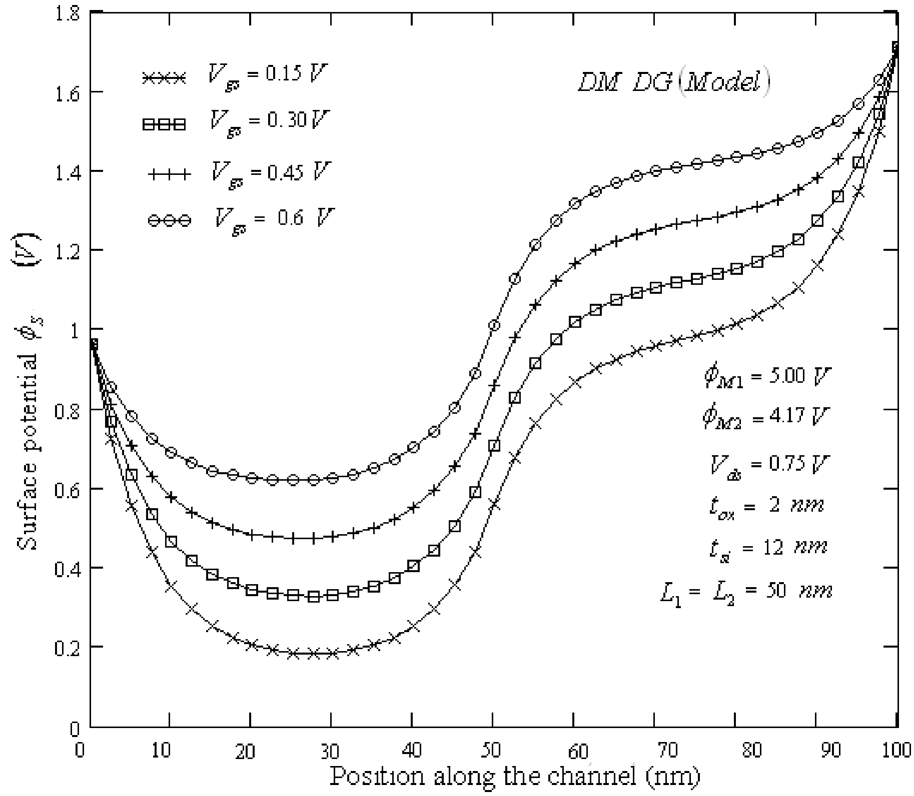

Fig 2.16 Potential profile at the surface of DM DG FD SOI MOSFET (Model) for a channel length L_g = 100nm for different values of V_{gs}.

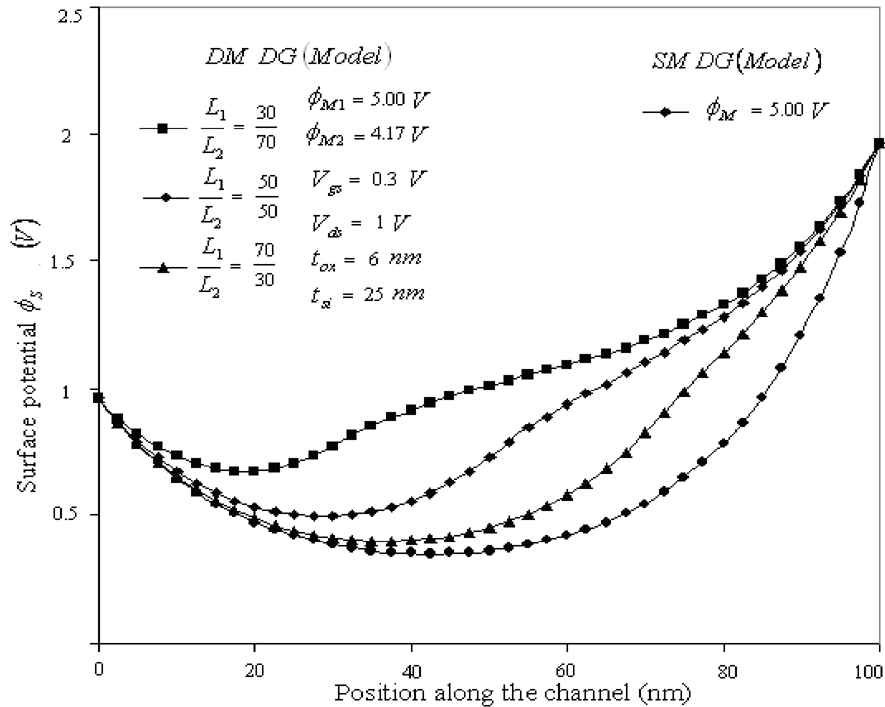

Fig 2.17 Potential profile at the surface of DM DG and SM DG FD SOI MOSFET (Model) for different combination of L_1 and L_2 keeping L_g = 100nm.

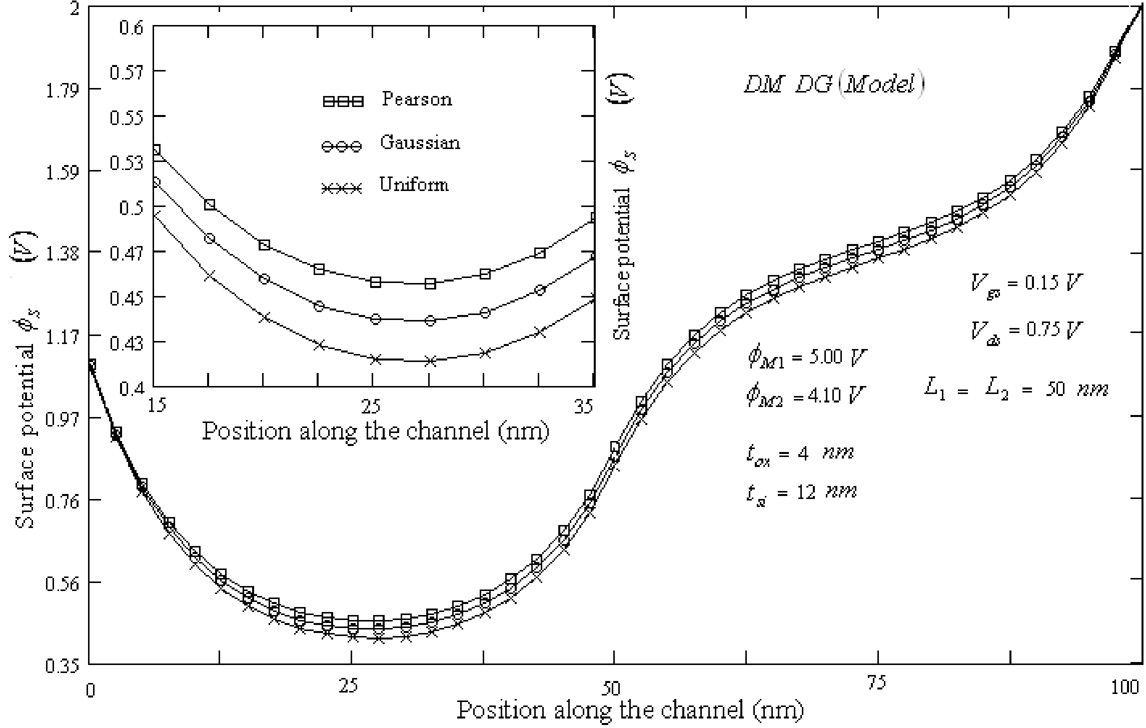

Fig 2.18 Variation of surface potential along the channel length in DM DG structure for three types of doping distributions.

2.4.1.3 Minimum Surface Potential and DIBL

The influence of *DIBL* on the subthreshold characteristic of the device is indicated by the position of minimum surface potential as the subthreshold leakage current often occurs at the position of minimum surface potential. The punch through occurs at minimum potential in the channel with $x = x_{\min}$ and is located under M1. Therefore at the point of minimum potential the electric field is assumed to be zero i.e.

From equation (2.54)
$$\left.\frac{d\phi_{f1}(x)}{dx}\right|_{x=x_{\min}} = 0 \tag{2.67}$$

$$\frac{d\phi_{f1}(x)}{dx} = -A_{011}.\frac{1}{\lambda_1}.\exp\left(\frac{-x}{\lambda_1}\right) + B_{011}.\frac{1}{\lambda_1}.\exp\left(\frac{x}{\lambda_1}\right)$$

$$\left.\frac{d\phi_{f1}(x)}{dx}\right|_{x=x_{\min}} = -A_{011}.\frac{1}{\lambda_1}.\exp\left(\frac{-x_{\min}}{\lambda_1}\right) + B_{011}.\frac{1}{\lambda_1}.\exp\left(\frac{x_{\min}}{\lambda_1}\right) = 0 \tag{2.68}$$

$$\frac{A_{011}}{B_{011}} = \frac{\exp\left(\frac{x_{\min}}{\lambda_1}\right)}{\exp\left(\frac{-x_{\min}}{\lambda_1}\right)} \quad ;$$

$$\frac{A_{011}}{B_{011}} = \exp\left(\frac{2.x_{\min}}{\lambda_1}\right) \quad ;$$

$$\ln\left(\frac{A_{011}}{B_{011}}\right) = \frac{2.x_{\min}}{\lambda_1} \; ;$$

$$x_{\min} = -\frac{\lambda_1}{2}\ln\left(\frac{A_{011}}{B_{011}}\right) \tag{2.69}$$

The minimum surface potential as well as potential at the center is obtained from equations (2.56) and (2.58). It is shown in figure 2.19 for different values of V_{ds}.

$$\phi_{c1}(x_{\min}) = \left((1+A_1)V'_{gs1} - A_1.V'_{gs11}\right) - \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^2 + A_{011}.\exp\left(\frac{x_{\min}}{\lambda_1}\right) + B_{011}.\exp\left(\frac{-x_{\min}}{\lambda_1}\right) \tag{2.70}$$

$$\phi_{s1}(x_{\min}) = \frac{1}{1+A_1}\left(\left((1+A_1)V'_{gs1}\right) - \frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^2 + A_{011}.\exp\left(\frac{x_{\min}}{\lambda_1}\right) + B_{011}.\exp\left(\frac{-x_{\min}}{\lambda_1}\right)\right) \tag{2.71}$$

Figure 2.19 shows the variation of surface potential of *DM DG FD* and *SM DG FD SOI MOSFET* for minimum value, along the channel length L_g, under M1 for different values of V_{ds}. It is observed that there is a continuous shift in the position of minimum surface potential while we increase the V_{ds} from 0.5 V to 1.5 V in case of *SM DG SOI MOSFET*. However in case of *DM DG SOI MOSFET*, the position of minimum surface potential remains constant with variation of V_{ds}. This indicates that the effect of *DIBL* is considerably reduced in *DM DG SOI* device as compared to *SM DG SOI* device because M2 region screens M1 region from any drain potential variation.

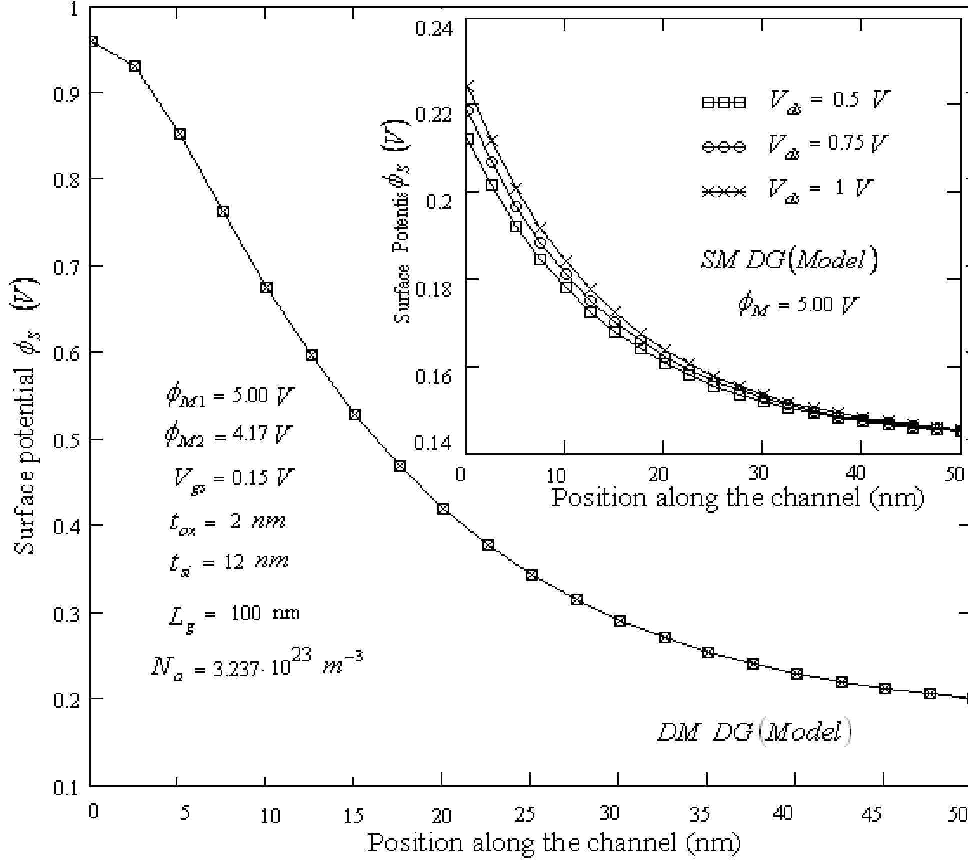

Fig 2.19 Minimum surface potential under M1 for different values of $V_{ds,}$ in SM DG and DM DG structures

2.4.1 Electric Field Distribution

The electric field distribution along the channel length (in the x-direction), can be calculated by differentiating the surface potential (equations 2.58 & 2.59), is given as

$$E_{s1}(x) = \left.\frac{\partial\phi_1(x,y)}{\partial x}\right|_{y=0}$$

$$= \frac{d\phi_{S1}(x)}{dx} = \frac{1}{(1+A_1)}.\left(\frac{A_{011}}{\lambda_1}.\exp\left(\frac{x}{\lambda_1}\right)+\frac{(-B_{011})}{\lambda_1}.\exp\left(\frac{-x}{\lambda_1}\right)\right)$$

$$\text{for } 0 \le x \le L_1 \text{ under M1} \tag{2.72}$$

$$E_{s2}(x) = \left.\frac{\partial \phi_2(x,y)}{\partial x}\right|_{y=0}$$

$$= \frac{d\phi_{S2}(x)}{dx} = \frac{1}{(1+A_1)}.\left(\frac{A_{022}}{\lambda_1}.\exp\left(\frac{x-L_1}{\lambda_1}\right) + \frac{(-B_{022})}{\lambda_1}.\exp\left(\frac{-(x-L_1)}{\lambda_1}\right)\right)$$

$$\text{for } L_1 \le x \le L_1 + L_2 \text{ under M2} \qquad (2.73)$$

Figure 2.20 shows the electric field variation along the channel length i.e. for $0 \le x \le L_g$ under M1 and M2. There is a peak electric field at the interface of M1 and M2. This peak electric field is responsible for higher carrier drift velocity and higher speed in *DM DG SOI* device. As the surface potential and center potential (equation (2.36)) are related, the electric field calculated from the center potential of the *DM DG* structure is also plotted. The results shown in figure 2.20 were obtained using the analytical model proposed in this work.

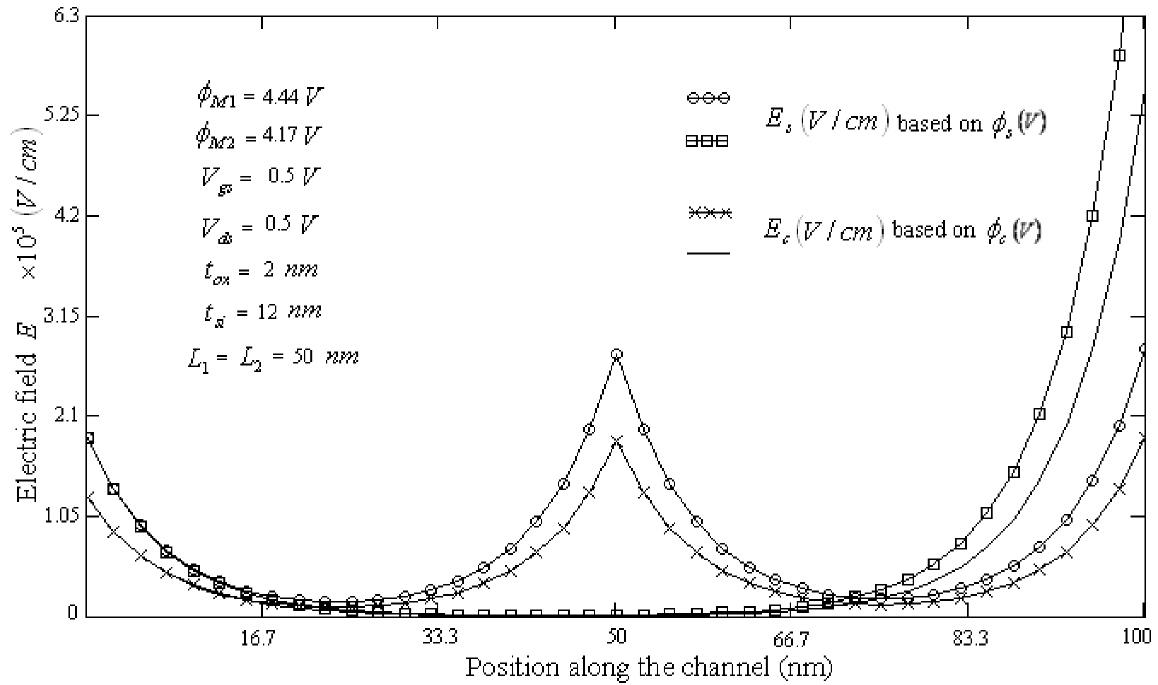

Fig 2.20 Electric field along the channel for (a) surface potential, E_s(V/cm) and (b) potential at the center, E_c(V/cm) in DM DG and SM DG SOI structures. For SM DG $\phi_M = 4.44$V.

The electric field based on surface potential for *DM DG SOI* as computed using the analytical model and also by device simulator is plotted in figure 2.21. It is shown that

the results obtained using the proposed analytical model is in excellent agreement with the same obtained using device simulator *ATLAS*.

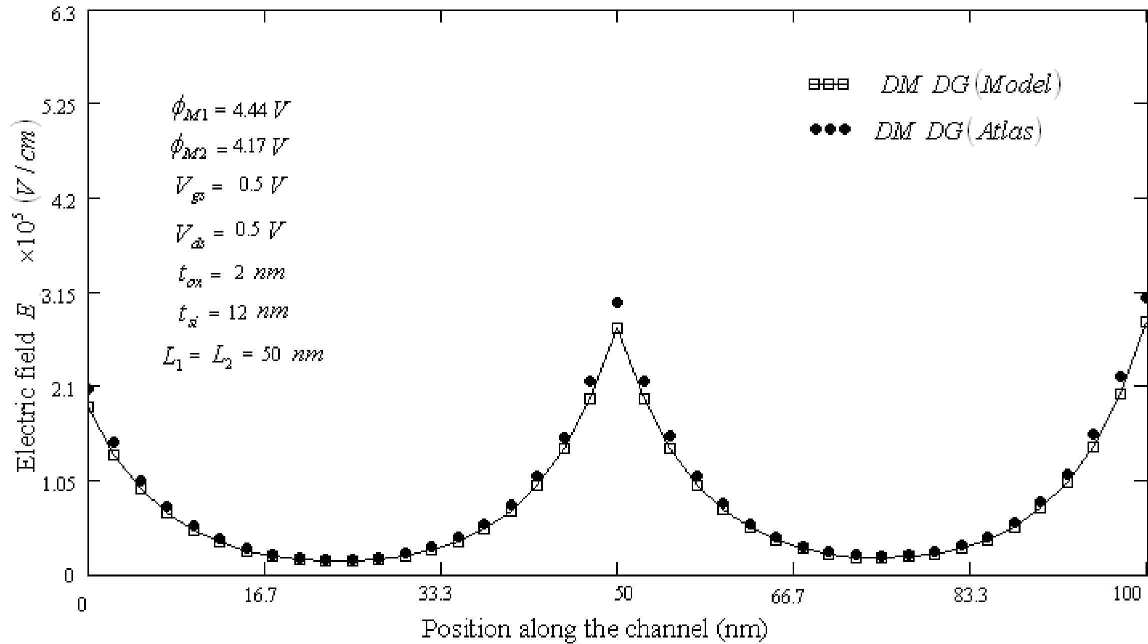

Fig 2.21 Electric field along the channel based on surface potential, E_s(V/cm) in DM DG SOI structure and its comparison with simulated values.

Figure 2.22 shows the variation of electric field based on surface potential along the channel length for different t_{ox}. It is observed that as the oxide thickness decreases the peak electric field at the interface of M1 & M2 increases due to the increase in transverse electric field, thereby increasing the average electric field in the channel.

When t_{ox} increases, the electric field discontinuity at the interface of the two gate metals causes the overall channel field to be flattened, increased at the source side, resulting in larger average velocity when the electrons enter into the channel from the source end.

Figure 2.23 shows the variation of the electric field based on surface potential of *DM DG SOI* device for different work function differences. It is observed that as the work function difference increases the electric field decreases at the drain end thereby causing a reduction in the hot-carrier effects.

Figure 2.24 shows the variation of electric field along the channel length for three types of doping distributions. It is observed that electric field is lowest at the drain end in case

of Pearson-IV type doping distribution indicating better screening of source if the doping distribution is Pearson IV type.

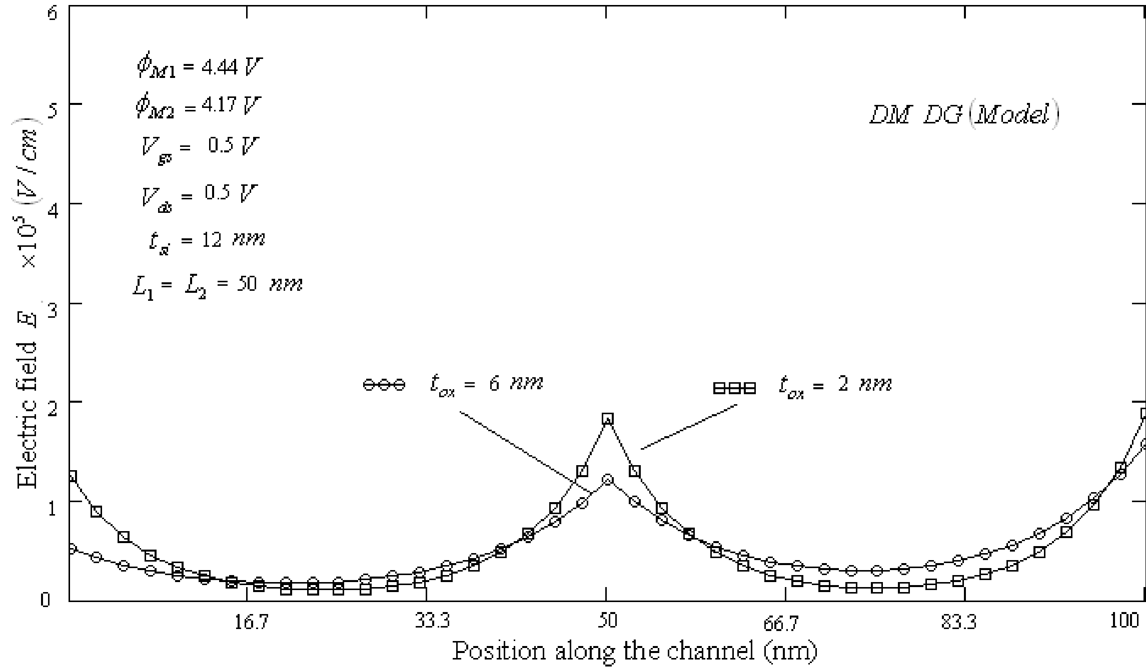

Fig 2.22 Electric field along the channel based on surface potential in DM DG SOI device for different t_{ox}.

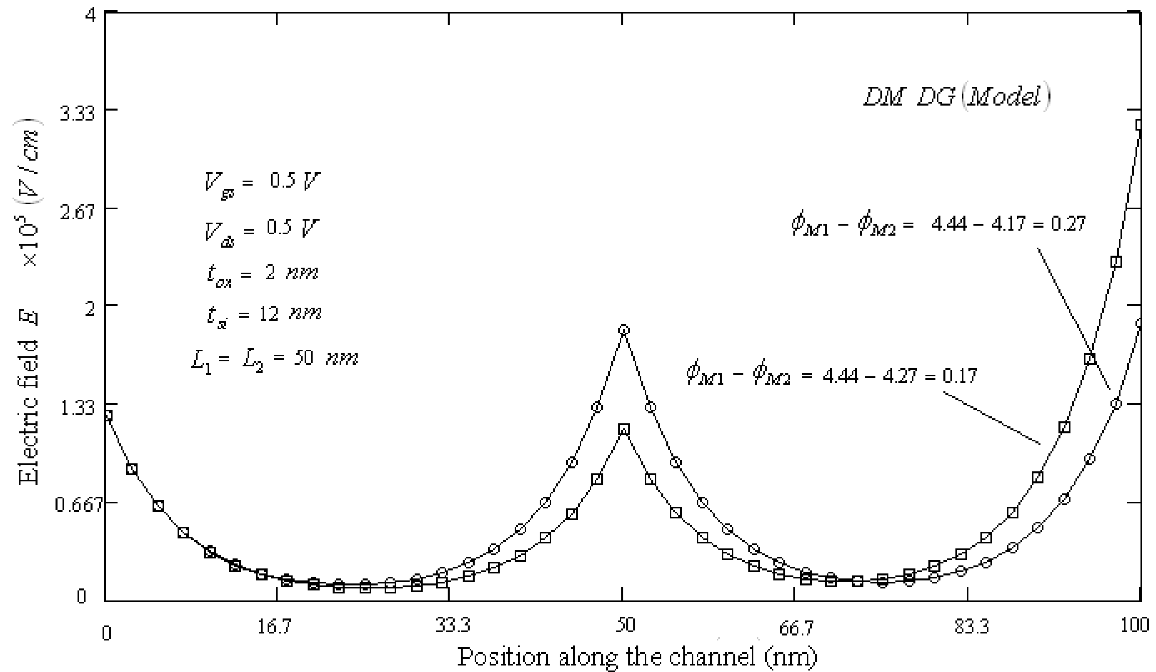

Fig 2.23 Electric field along the channel based on surface potential in DM DG SOI device for different work function differences.

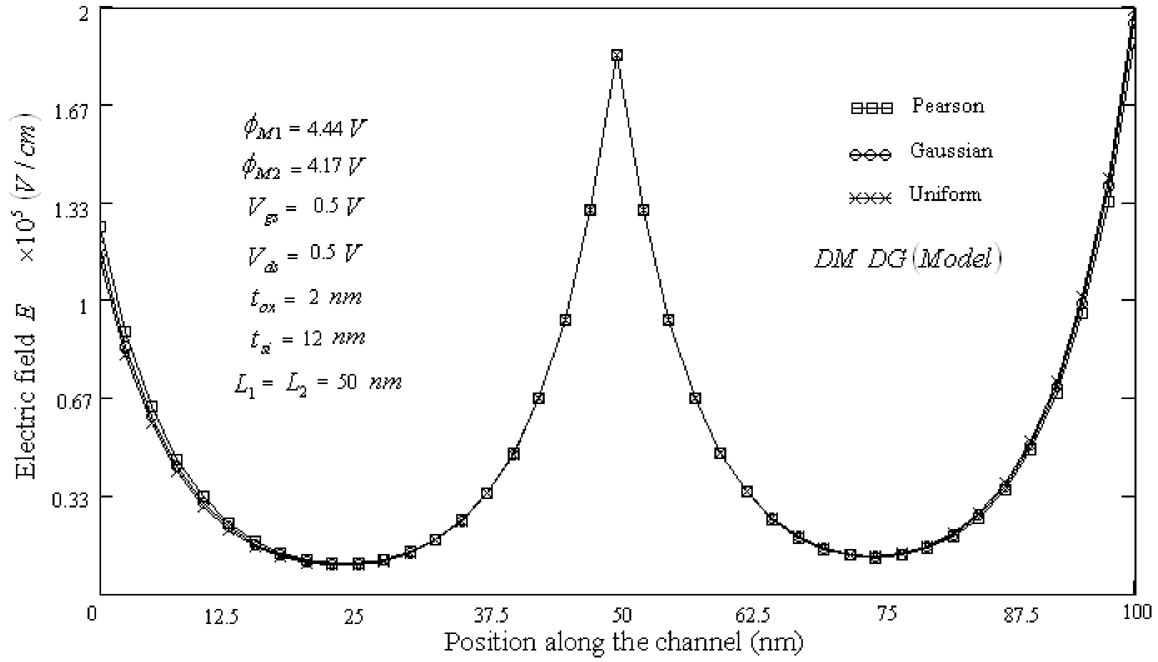

Fig 2.24 Electric field along the channel in DM DG SOI device for three types of doping distribution.

2.5 Electron Velocity Distribution

In order to explain the electron transport efficiency (also called gate transport efficiency) of *DM DG* structure, the electron / hole velocity distribution for *n*-channel (*p*-channel) *MOSFET* is very important. It is given as [94]

$$v_{s1}(x) = 1.07\times10^7 . \frac{E_{s1}(x)/6.91\times10^3}{\left[1+\left(E_{s1}(x)/6.91\times10^3\right)^{1.11}\right]^{\frac{1}{1.11}}} \text{ for } 0 \le x \le L_1 \text{ under M1} \tag{2.74}$$

$$v_{s2}(x) = 1.07\times10^7 . \frac{E_{s2}(x)/6.91\times10^3}{\left[1+\left(E_{s2}(x)/6.91\times10^3\right)^{1.11}\right]^{\frac{1}{1.11}}} \text{ for } L_1 \le x \le L_1+L_2 \text{ under M2} \tag{2.75}$$

Figure 2.25 and 2.26 show the variation of electron velocity along the channel between model and simulator results for DM DG structure. It is observed that the electron velocity under M2 is increasing more as compared to the electron velocity under M1 when the metal workfunction difference is less i.e. $\phi_{M1} - \phi_{M2} = 4.44 - 4.17 = 0.27V$ and as the

metal workfunction difference increases as shown in figure 2.26, the electron velocity, at the drain end, decreases leading to reduction in hot-electron effect.

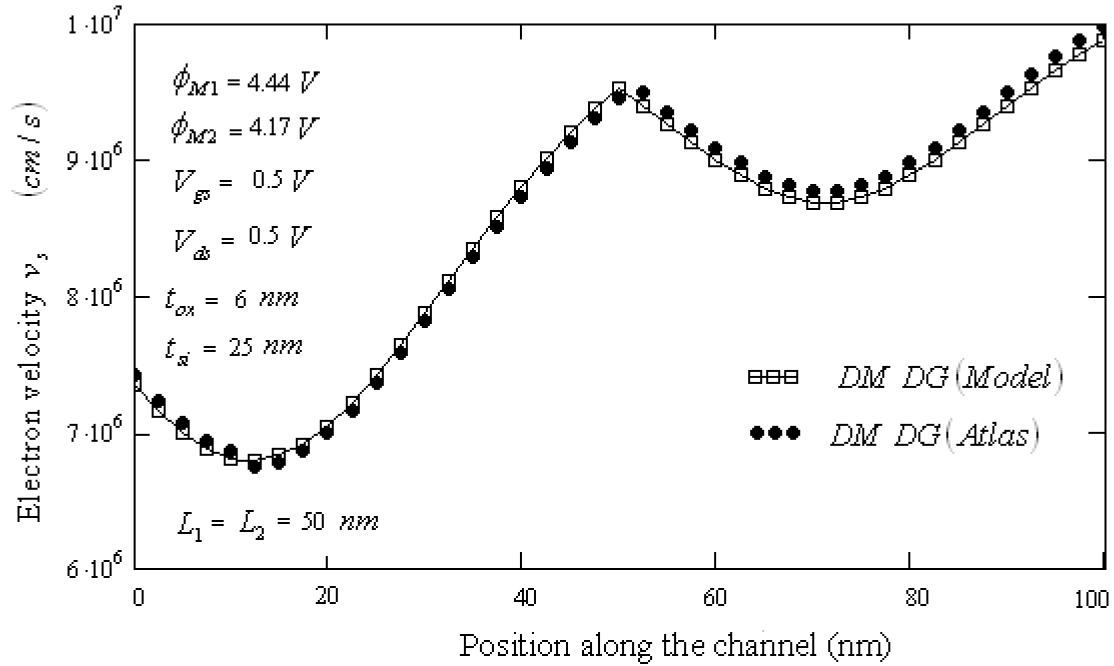

Fig 2.25 Electron velocity along the channel in DM DG SOI structure (model and simulator).

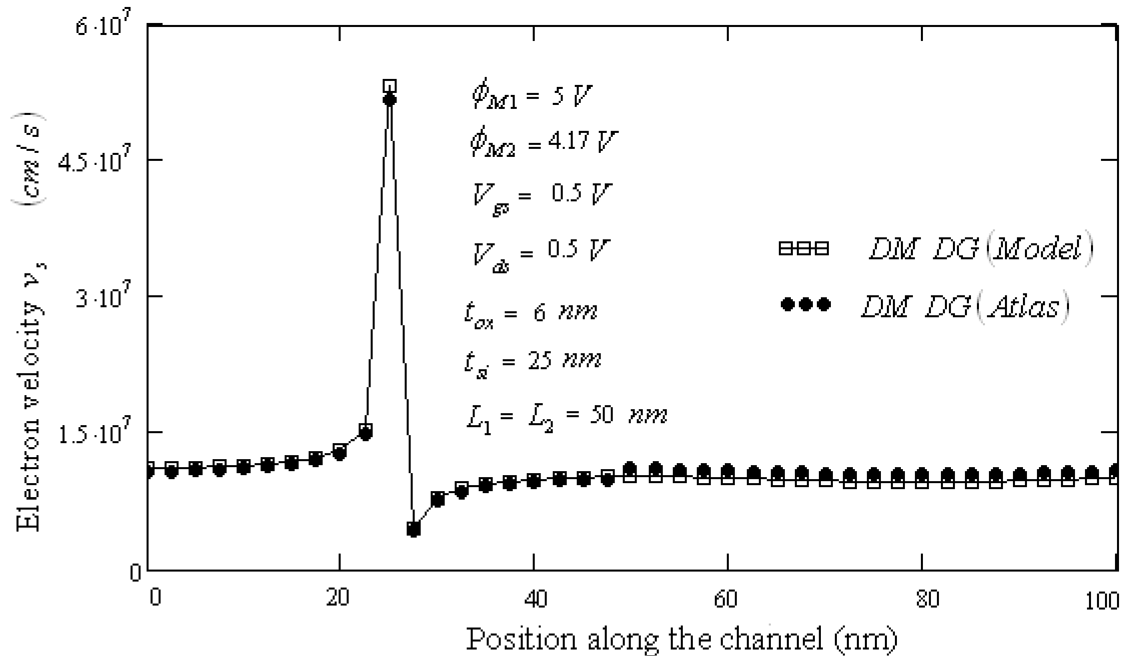

Fig 2.26 Electron velocity along the channel in DM DG SOI structure (model and simulator) on $\phi_{M1} = 5.00V$ and $\phi_{M2} = 4.17V$.

2.6 Subthreshold Swing

The subthreshold swing which indicates the extent of coupling between the gate and the channel in Dual-Material *DG FD SOI MOSFET* is given as

$$S = \frac{\ln 10}{\beta} \times \frac{1}{\dfrac{d\phi_s(x_{\min})}{dV_{gs}}} \tag{2.76}$$

where $\beta = \frac{q}{kT}$ and $\frac{d\phi_s(x_{\min})}{dV_{gs}}$ is obtained on differentiating equation (2.70) w.r.t. V_{gs}, which is given by

$$\frac{d\phi_c(x_{\min})}{dV_{gs}} = 1 + \frac{1}{E_1}\left(\frac{C_{011}.\exp\left(\frac{-1}{2}\right)}{.(B_{011})^2} + (1+A_1).\left(\exp\left(\frac{-L_1}{\lambda_1}\right) - \exp\left(\frac{L_2}{\lambda_1}\right)\right)\exp\left(\frac{1}{2}\right)\right) \tag{2.77}$$

here $E_1 = \left(\exp\left(\frac{L_1 + 2L_2}{\lambda_1}\right) - \exp\left(-\frac{L_1}{\lambda_1}\right)\right)$ and

$$C_{011} = -2.B_{011}.A_{011}.\left(\exp\left(\frac{L_2}{\lambda_1}\right) - \exp\left(\frac{-L_1}{\lambda_1}\right)\right).(1+A_1) - (A_{011})^2.(1+A_1).\left(\exp\left(\frac{L_2}{\lambda_1}\right) - \exp\left(\frac{L_1 + 2.L_2}{\lambda_1}\right)\right)$$

And as we know, $\frac{d\phi_s(x)}{dV_{gs}} = (1+A_1)^{-1}.\left(\frac{d\phi_c(x)}{dV_{gs}} + A_1\right)$

Figure 2.27 shows the variation of subthreshold swing along the channel for *DM DG* as well as *SM DG* structure. It is observed that there is no significant change in subthreshold swing for *DM DG* and *SM DG* structures. This is because of less change in surface potential over change in gate to source voltage.

Figure 2.28 shows the subthreshold swing based on surface potential for *DM DG SOI* as computed using the analytical model and also by device simulator. It is shown that the results obtained (figure 2.28) using the proposed analytical model is in excellent agreement with the same obtained using device simulator *ATLAS*.

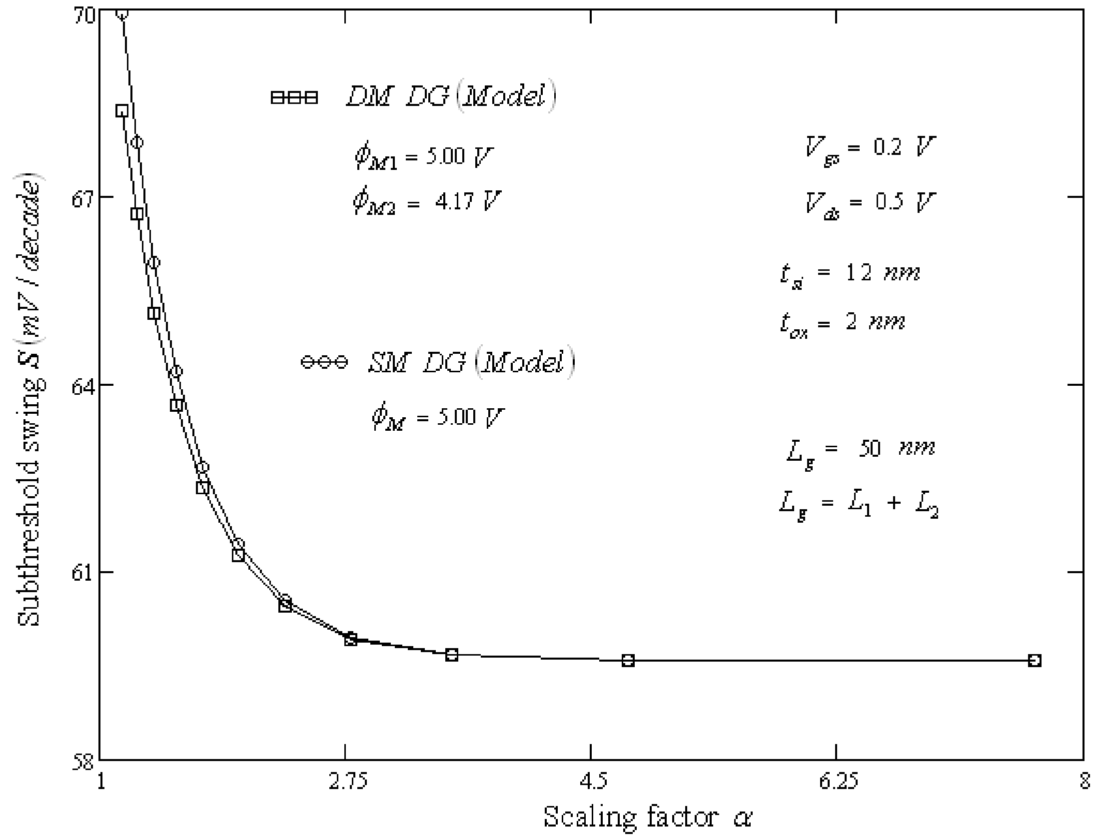

Fig 2.27 Comparison in DM DG and SM DG structures for subthreshold swing.

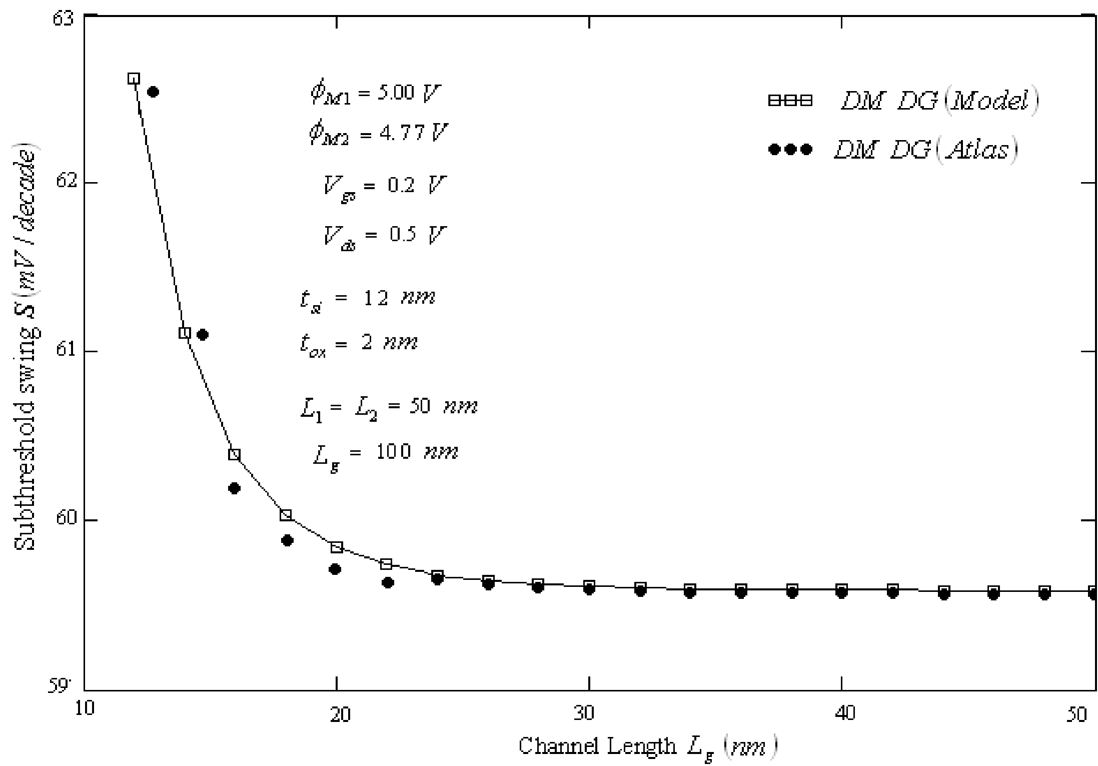

Fig 2.28 Comparison in analytical DM DG model and simulated model for subthreshold swing.

2.7 Summary

A *2D* analytical model for Dual-Material Double-Gate Fully-Depleted *SOI-MOSFET* with Pearson IV type doping distribution has been proposed for computing potential and electric field distribution. The potential and electric field distribution have been obtained using the analytical model and also using the device simulator *ATLAS* (using numerical analysis). The results obtained using two approaches have been found to be in excellent agreement.

It has been shown that

1. In case of *DM DG SOI MOSFET*, the source is effectively screen from the variation in the drain voltage due to step function profile of the potential at the interface of metals M1 and M2.
2. It has been observed that there is a continuous shift in the position of minimum surface potential while we increase the V_{ds} from 0.5 V to 1.5 V in case of *SM DG SOI MOSFET*. However in case of *DM DG SOI MOSFET*, the position of minimum surface potential remains constant with variation of V_{ds}.
3. It has been shown that the effect of *DIBL* is considerably reduced in case of *DM DG SOI MOSFET* but at the same time subthreshold swing shows less significant improvements.
4. In case of *DM DG SOI MOSFET*, the electric field is reduced near the drain leading to reduction in hot carrier effect. The reduction in electric field near the drain is also found to be dependent upon the difference between the work function of the two metals. As the difference between the work functions of the two metal decreases the electric field near the drain increases.
5. In *DM DG SOI MOSFET*, as the metal workfunction difference increases the electron velocity, at the drain end, decreases leading to reduction in hot-electron effect.
6. The nature of impurity distribution is also significantly affects the potential and electric field distribution and therefore the device characteristics.

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Chapter-III

SWITCHING CHARACTERISTICS OF n-CHANNEL DM DG FD SOI MOSFET

3.1 Introduction

In this chapter, the analytical expressions for the following device parameters (relevant to the switching behavior of the *MOSFET*) have been derived for the basic physical consideration using approximate boundary conditions.

1	Threshold voltage	5	Drain resistance
2	Device capacitance	6	Cut-off frequency
3	Drain current	7	Transit time
4	Transconductance	8	Noise- Thermal and Flicker Noise

3.2 Threshold Voltage

The threshold voltage can be defined as gate voltage for which the minimum surface potential is twice the Fermi potential. Since the same metals are used on both the gates, the threshold voltages on both the gates are equal. Substituting $\phi_{s1}\left(x_{\min},\frac{t_{si}}{2}\right)=2.\phi_F$ and $V_{gs}=V_{th}$ into equation (2.71), the threshold voltage obtained is given as

$$V_{th}=\frac{-G7+\sqrt{G7^2-4.G6.G8}}{2.G6} \quad (3.1)$$

The derivation of the above equation and the expressions of $G7, G6$ and $G8$ are given in *Appendix: D*. In *DM DG SOI* structure, the position of x_{min} lies under the metal gate M1 (both side) because $V_{FB1} > V_{FB2}$ and therefore, the effective gate voltage under the M1 region is less than that for M2. Figure 3.1 shows the variation of threshold voltage of *DM DG* and *SM DG* structure along the channel length under L_2 for fixed value of $L_1 = 50$ *nm*. It is observed that the threshold voltage rolls up in case of *DM DG SOI* structure in comparison to the rolls down for *SM DG SOI* structure with decreasing channel length. It is because of increasing L_1/L_2 ratio and increasing portion of the larger work function

gate as the channel length reduces. This is a unique feature which gives *DM DG* structure an added advantage when the device dimensions are continuously shrinking. It can also be seen in figure 3.2 that the threshold voltage as calculated using analytical equation (3.1) is in close agreement with the same computed using device simulator *ATLAS*. Except this roll up, the threshold voltage of the *DM DG* structure is about the same as a *SM DG* structure having the same gate material as M1 of the *DM DG* structure. Therefore, the channel region under M2 has more freedom of optimization. For instance, the substrate doping of this region can be reduced, thereby it has added advantage that source and drain capacitance can be decreased, while potentially improving the speed over the conventional device.

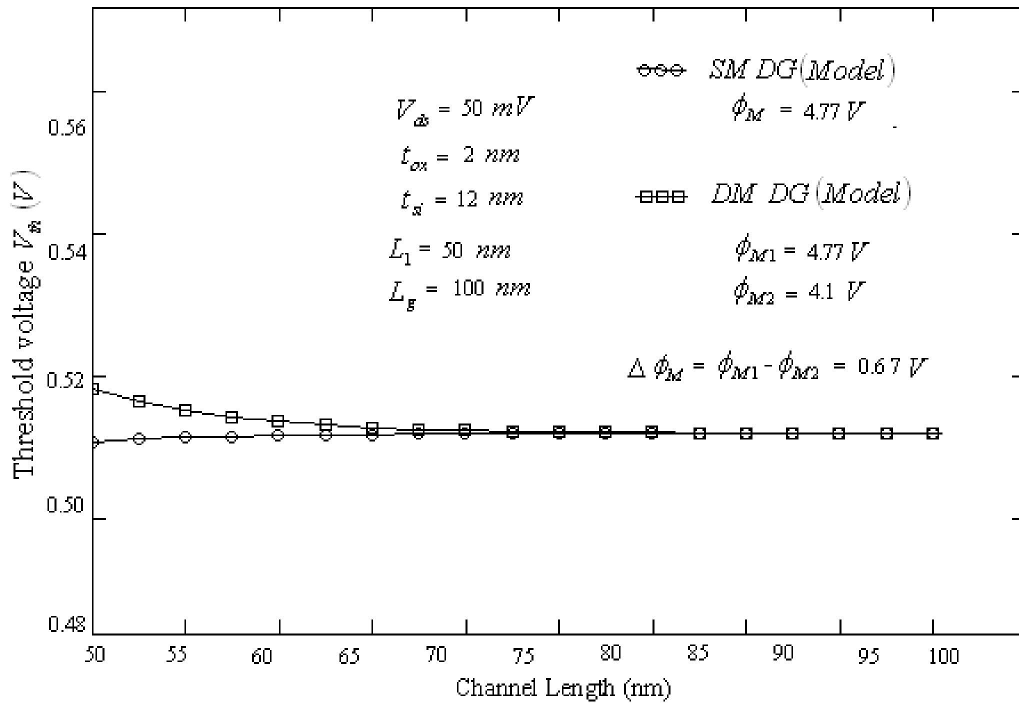

Fig 3.1 Threshold voltage along the channel for fixed L_1 = 50 nm in SM DG and DM DG structures.

When the difference between the work function of M1 and M2 changes, the threshold voltage also changes, as shown in figure 3.3. From figure 3.2 and figure 3.3, it is evident that if the work function difference increases the threshold voltage also increases, as predicted by equation (3.1). When the device is on then the screen gate shields the region under the control gate from any drain voltage variations and in this way, screen gate absorbs any additional drain to source voltage beyond saturation. This in turns leads to reduction in *DIBL*.

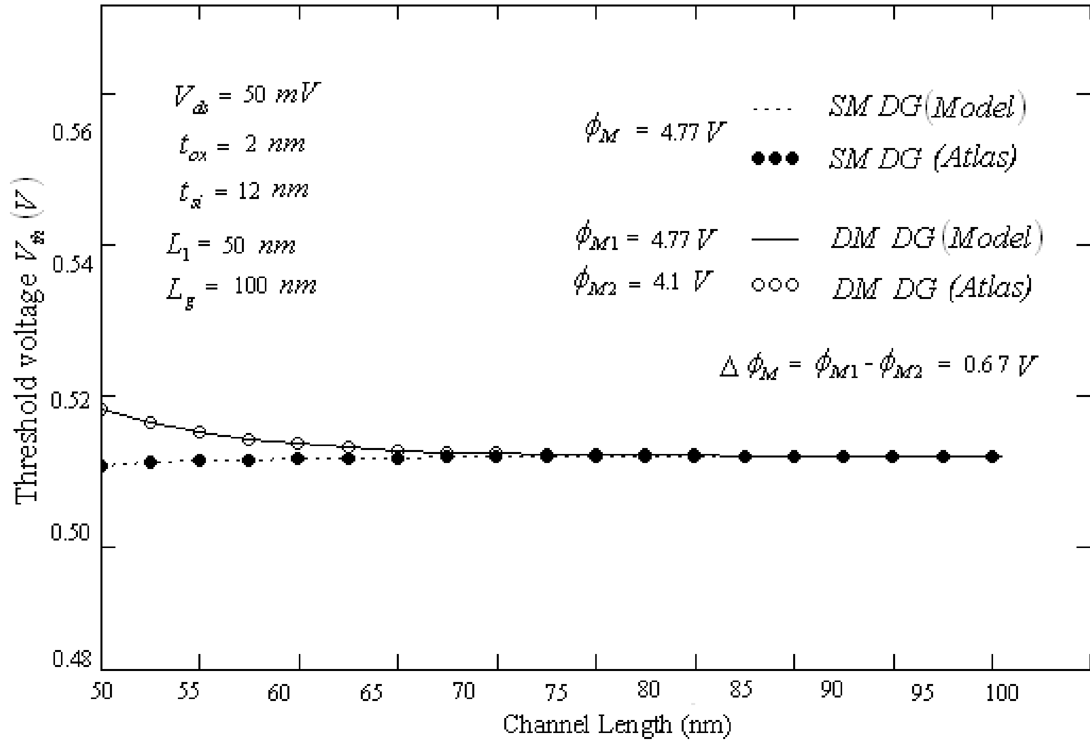

Fig 3.2 Comparison of analytical model with simulated values of threshold voltage for fixed L_1 = 50 nm in SM DG and DM DG structures.

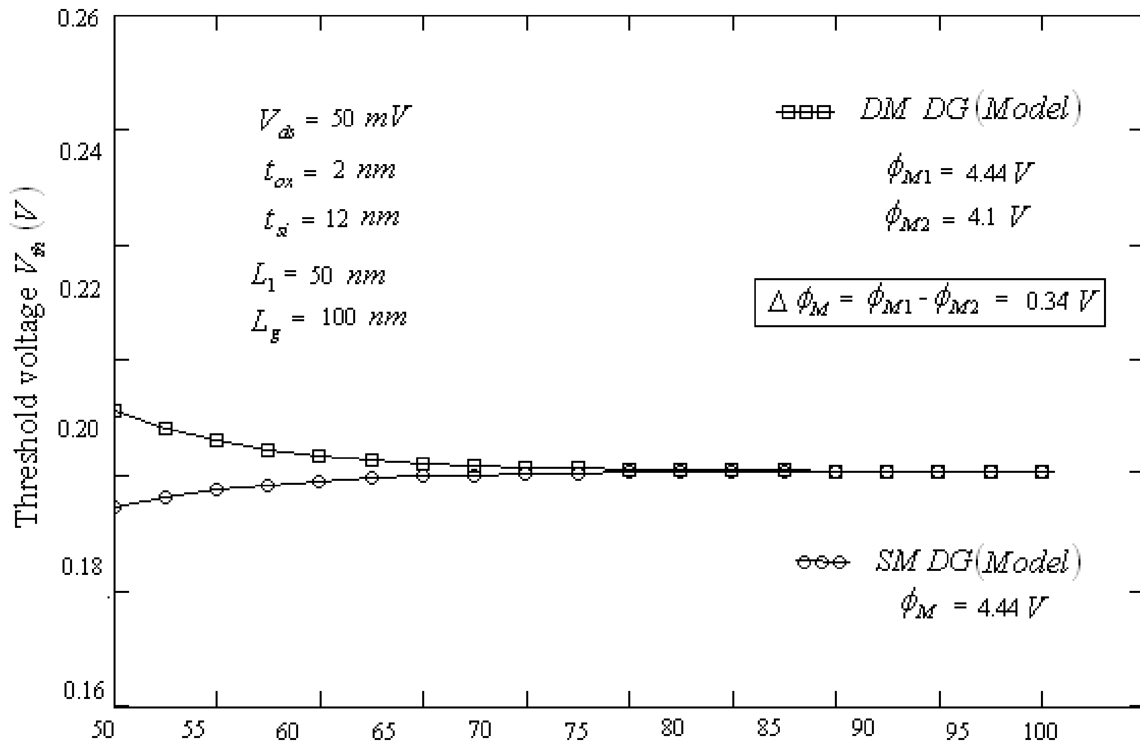

Fig 3.3 Threshold voltage along the channel for fixed L_1 = 50 nm in SM DG and DM DG structures for different work functions.

Figure 3.4 shows the variation of threshold voltage along the channel under M2 for different doping distribution profiles keeping the dose constant. It is observed that the threshold voltage is significantly reduced when doping distribution is Pearson IV type.

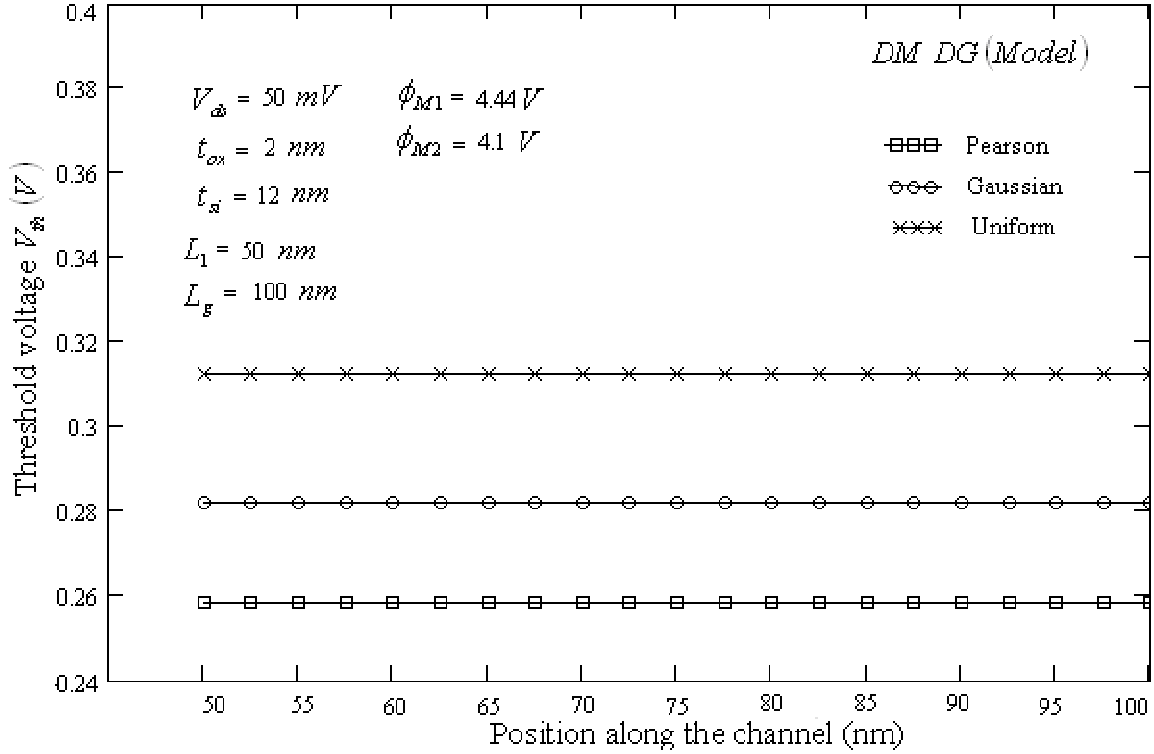

Fig 3.4 Threshold voltage along the channel in DM DG structure for different doping distribution.

3.3 Device Capacitance

The equivalent circuit of *DM DG FD SOI MOSFET,* ignoring the resistance, is shown in figure 3.5 (a). Here $C_{GS} = C_{SG} = C_{GD} = C_{DG}$ as the device is symmetric.

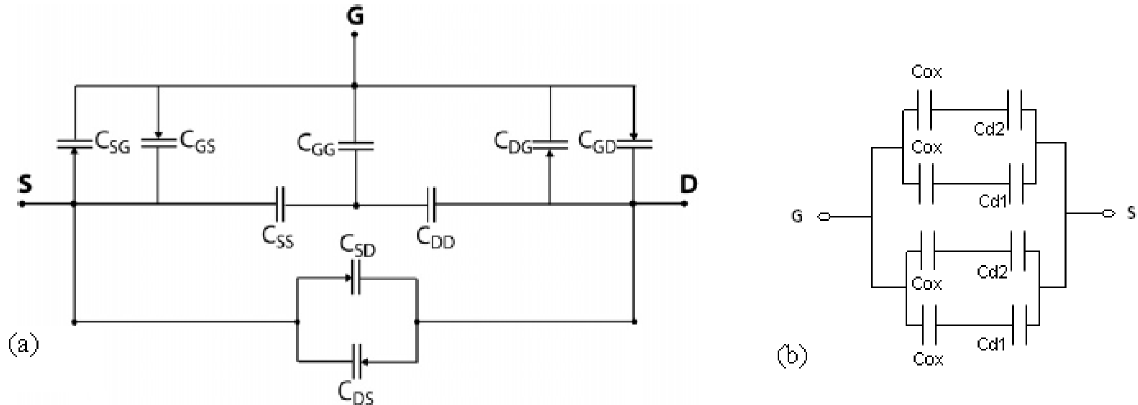

Fig 3.5 (a) Equivalent circuit of DM DG FD SOI MOSFET and (b) Simplified circuit for C_{GS}.

In figure 3.5, C_{GS} is gate-source trans capacitance, similarly, C_{GD}, C_{SG} and C_{DG} are gate-drain, source-gate and drain-gate capacitance. C_{SS} and C_{DD} are source and drain self capacitances. In a *DG SOI MOSFET,* the depletion regions charge under M1 and M2 [96, 94] are given by

$$Q_{d1} = \sqrt{2.q.N_a\left(\frac{t_{si}}{2}\right).\varepsilon_{si}}.\sqrt{\phi_{s1}(x)} \quad \text{for} \quad 0 \le x \le L_1 \tag{3.2}$$

and $$Q_{d2} = \sqrt{2.q.N_a\left(\frac{t_{si}}{2}\right).\varepsilon_{si}}.\sqrt{\phi_{s2}(x)} \quad \text{for} \quad L_1 \le x \le L_1 + L_2 \tag{3.3}$$

Here $N_a\left(\frac{t_{si}}{2}\right)$ is the doping concentration, calculated at $y = \frac{t_{si}}{2}$. The different capacitances associated are obtained as follows:

(a) The depletion layer capacitance is the rate of change of depletion layer charge with gate voltage and is given by

$$C_{d1} = \frac{dQ_{d1}}{dV_{gs}} = \sqrt{\frac{q.N_a\left(\frac{t_{si}}{2}\right).\varepsilon_{si}}{2.\phi_{s1}(x)}}.\frac{d\phi_{s1}(x)}{dV_{gs}} \tag{3.4}$$

and $$C_{d2} = \frac{dQ_{d2}}{dV_{gs}} = \sqrt{\frac{q.N_a\left(\frac{t_{si}}{2}\right).\varepsilon_{si}}{2.\phi_{s2}(x)}}.\frac{d\phi_{s2}(x)}{dV_{gs}} \tag{3.5}$$

where

$$\frac{d\phi_{s1}(x)}{dV_{gs}} = 1 + \frac{E_2 - E_3}{E_1}.\exp\left(\frac{x}{\lambda_1}\right) + \frac{E_3 - E_5}{E_1}.\exp\left(-\frac{x}{\lambda_1}\right) \quad \text{for} \quad 0 \le x \le L_1 \tag{3.6}$$

and $$\frac{d\phi_{s2}(x)}{dV_{gs}} = 1 + \frac{(C_1 + C_2)}{C_5}.\exp\left(\frac{x - L_1}{\lambda_1}\right) + \frac{C_3 + C_4}{C_5}.\exp\left(-\frac{(x - L_1)}{\lambda_1}\right)\exp\left(\frac{L_2}{\lambda_1}\right)$$

$$\text{for } L_1 \le x \le L_1 + L_2 \tag{3.7}$$

here $E_1 = \exp\left(\frac{L_g + L_2}{\lambda_1}\right) - \exp\left(\frac{-L_g + L_2}{\lambda_1}\right)$; $E_2 = \exp\left(\frac{-L_g + L_2}{\lambda}\right)$;

$E_3 = \exp\left(\frac{L_g - L_1}{\lambda}\right)$; $E_5 = \exp\left(\frac{L_g + L_2}{\lambda}\right)$

$$C_1 = -1 + \exp\left(\frac{2.L_2}{\lambda_1}\right); \qquad C_2 = \exp\left(\frac{L_1 + L_2}{\lambda_1}\right) - \exp\left(\frac{L_1 + 3.L_2}{\lambda_1}\right)$$

$$C_3 = -\exp\left(-\frac{L_1}{\lambda_1}\right) + \exp\left(-\frac{L_1 - 2.L_2}{\lambda_1}\right); \qquad C_4 = \exp\left(\frac{L_2}{\lambda_1}\right) - \exp\left(\frac{3.L_2}{\lambda_1}\right);$$

$$C_5 = \left(\exp\left(\frac{L_1 + 2L_2}{\lambda_1}\right) - \exp\left(-\frac{L_1}{\lambda_1}\right)\right)\left(-1 + \exp\left(\frac{2L_2}{\lambda_1}\right)\right)$$

Using equation (2.36), which relates $\phi_s(x)$ and $\phi_c(x)$, it is possible to express the depletion layer capacitance in terms of $\phi_c(x)$, where $\frac{d\phi_{c1}(x)}{dV_{gs}}$ and $\frac{d\phi_{c2}(x)}{dV_{gs}}$ are given as

$$\frac{d\phi_{c1}(x)}{dV_{gs}} = (1 + A_1).\frac{d\phi_{s1}(x)}{dV_{gs}} - A_1 \text{ and} \tag{3.8}$$

$$\frac{d\phi_{c2}(x)}{dV_{gs}} = (1 + A_1).\frac{d\phi_{s2}(x)}{dV_{gs}} - A_1 \tag{3.9}$$

(b) The interface capacitance, C_{ss1} is given by

$C_{ss1} = q.N_{ss}$, where N_{ss} *(cm^{-1} eV^{-1})* is the interface state density.

(c) Gate to source capacitance, C_{GS} is given by

$$C_{GS} = 2.\frac{(C_{d2}.C_{ox}).(C_{d1} + C_{ox}) + (C_{d1}.C_{ox}).(C_{d2} + C_{ox}) + C_{ss1}.(C_{d2} + C_{ox}).(C_{d1} + C_{ox})}{(C_{d2} + C_{ox}).(C_{d1} + C_{ox})} \tag{3.10}$$

here $$C_{GS} = C_{SG} = C_{GD} = C_{DG} \tag{3.11}$$

The depletion layer capacitance of *DM DG FD SOI MOSFET* as a function of gate to source voltage for surface potential is shown in figure 3.6. Correspondingly, in figure 3.7, the device depletion capacitance is plotted as a function of gate to source voltage in *SM DG FD SOI MOSFET* also, using the analytical model. It is seen that the depletion capacitance is much larger in case *SM DG* structure particularly for a small value of gate to source voltage. This is expected because in *SM DG* structure the metal chosen had larger work function. In figure 3.8, the calculated value of the gate-source capacitance vs gate to source voltages as obtained using analytical model for *SM DG* and *DM DG* structures.

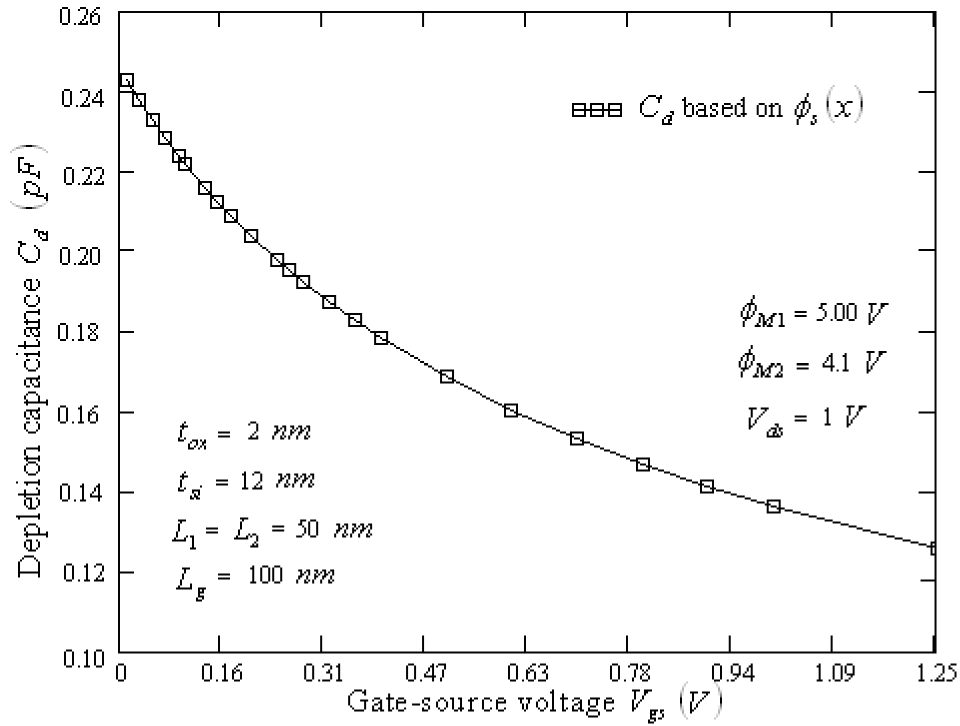

Fig 3.6 Depletion layer capacitance vs gate-source voltage based on surface potential.

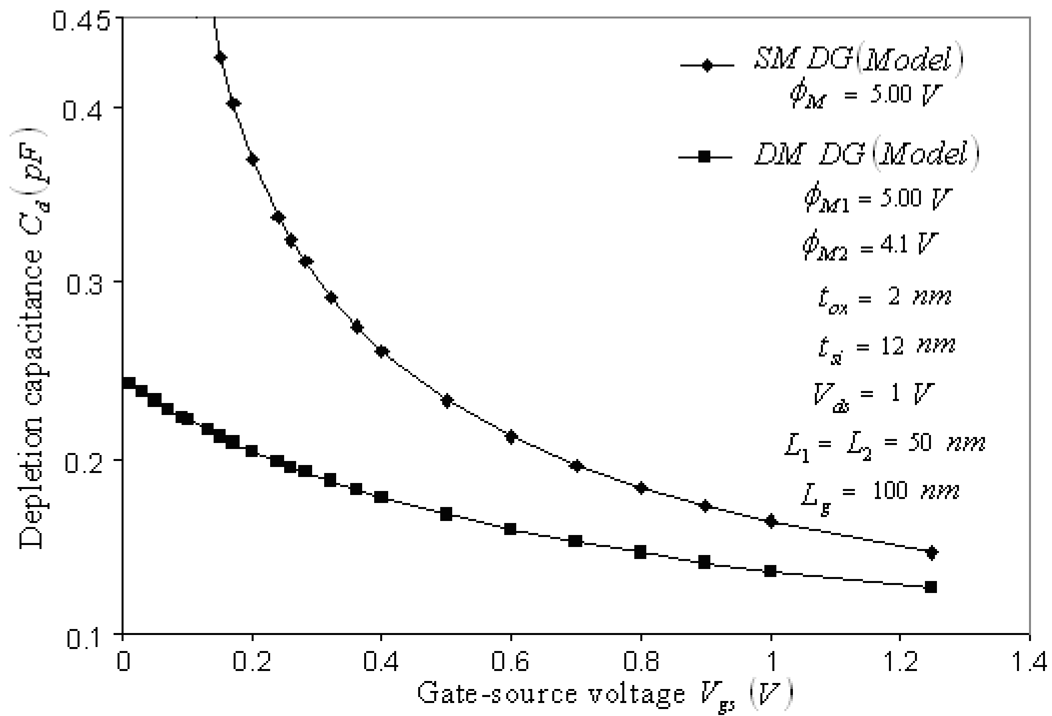

Fig 3.7 Depletion layer capacitance vs gate-to-source voltage in DM DG and SM DG structures.

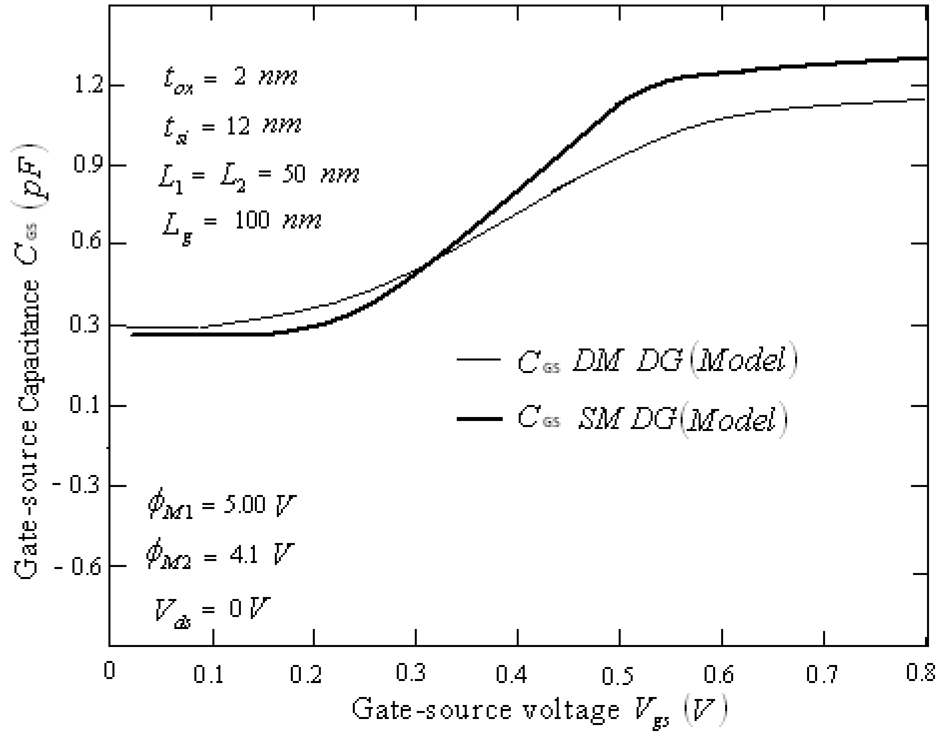

Fig 3.8 Gate-to-source capacitance vs gate-source voltage for DM DG and SM DG structures.

Figure 3.8 shows the C_{GS} is low in case of *DM DG* as compare to *SM DG* due to introduction of two metals in gate. Figure 3.9 shows the variation of the depletion capacitance with gate-to-source voltage for different doping distribution functions. It is seen that the depletion layer capacitance is low for devices having Pearson IV doping distribution.

The smaller value of depletion layer capacitance makes the device more useful for high speed as well as for the low power *VLSI* circuits. Because of the excess majority carriers accumulating under M1 and M2 of both sides of *DM DG FD SOI* structure, the depletion layer capacitances, C_{d1} and C_{d2}, due to V_{gs} -V_{fbf1} and V_{gs} -V_{fbf2}, becomes large. As the gate voltage further increases, the device capacitance decreases very fast.

The gate-to-source capacitance variation with respect to gate-to-source voltage for *DM DG FD SOI* structure is shown in figure 3.10. The results are shown to compare very well with simulations performed using the Silvaco Atlas device simulator.

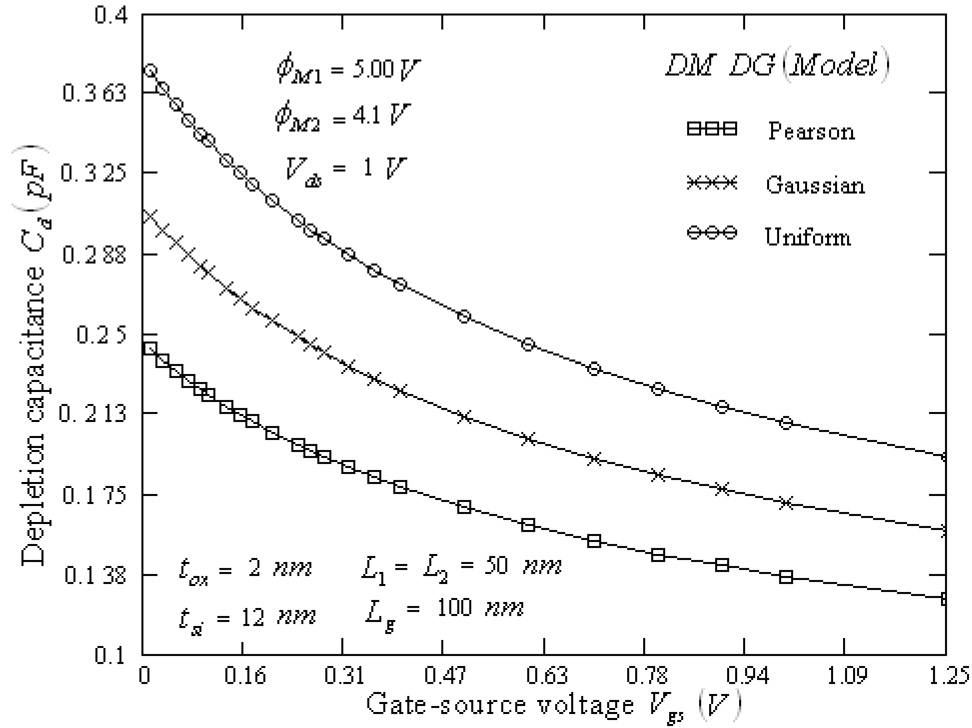

Fig 3.9 Depletion layer capacitance in DM DG structure for different doping distribution.

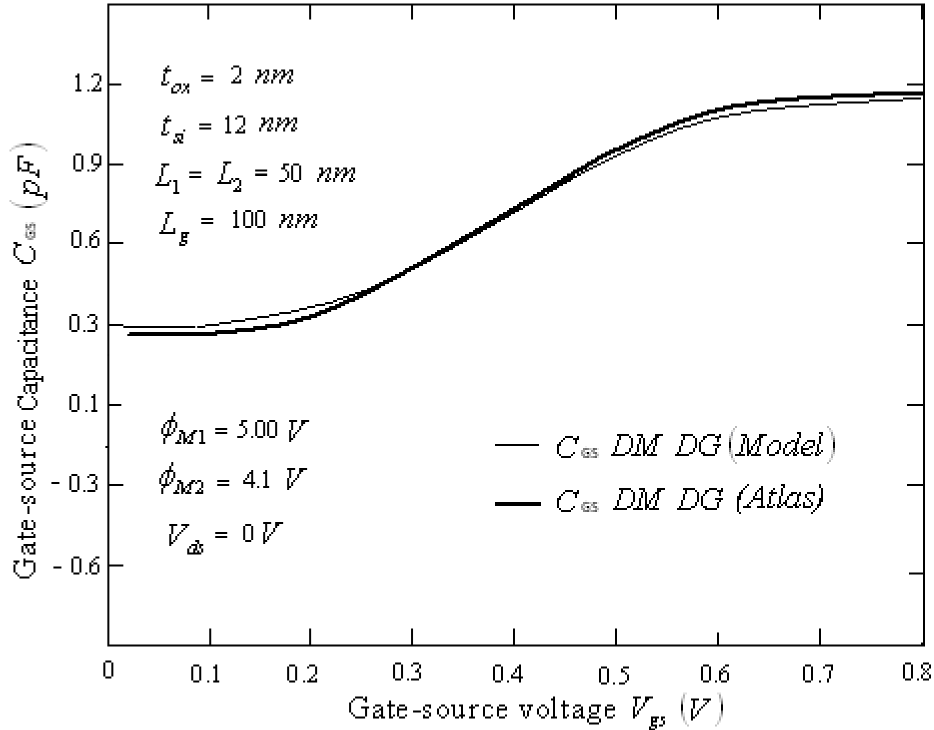

Fig 3.10 Gate-to-source capacitance in DM DG structure and its comparison with simulator's value.

3.4 Drain-Current Characteristics

The current-voltage characteristics may be derived keeping in view the position dependent inversion layer charge and field dependent electron mobility. For a strongly inverted *n*-channel enhancement mode dual-material double-gate fully-depleted *SOI MOSFET*, the drain currents are given by

$$I_{ds} = -W.\mu_n(x).Q_n(x).\frac{d\phi_c(x)}{dx} \quad \text{and} \tag{3.12}$$

$$= I_1 + I_2 \quad \text{--- say (Please see } \textit{Appendix: E}\text{)} \tag{3.13}$$

where I_{ds} is the drain current, $I_1 = -W.\mu_{n1}(x).Q_{n1}(x).\frac{d\phi_{c1}(x)}{dx}$, $I_2 = -W.\mu_{n2}(x).Q_{n2}(x).\frac{d\phi_{c2}(x)}{dx}$ and W is the gate-width. As our device is symmetric, $Q_n(x)$, the inversion layer charge, is double of carrier charge under each gate

$$Q_n(x) = 2.[Q_s(x) - Q_d] \tag{3.14}$$

Here, $Q_s(x)$ and Q_d are the surface charge and depletion layer charge densities. The surface charge is obtained using

$$Q_s(x) = -C_{ox}.[V_{gs} + V_{sub} - V_{fbf} - \phi_c(x)] \tag{3.15}$$

where C_{ox} is the oxide capacitance, V_{fbf} is the flat band voltage, V_{gs} is the applied gate-to-source voltage, $\phi_c(x)$ is the potential at the center of the channel and V_{sub} is the substrate potential. The depletion layer charge is given by

$$Q_d = C_{ox}.[V_{fbf} - V_{th} + \phi_F] \tag{3.16}$$

where V_{th} is the threshold voltage given by equation (3.1) and ϕ_F is the Fermi potential. The field dependent mobility of electrons in equations (3.12) is given by

$$\mu_n(x) = \frac{\mu_{no}}{\sqrt{1 + \left(\frac{E(x)}{E_c}\right)^2}} \tag{3.17}$$

where μ_{no} is the low field mobility, E_c is the critical field and $E(x)$ is the lateral field, given as

$$E(x)=\frac{C_{ox}.(V_{fbf}-V_{gs}+\phi_c(x))}{\varepsilon_{si}} \tag{3.18}$$

On substituting the values of $Q_n(x)$ and $\mu_n(x)$ in equation (3.12), we get

$$I_{ds} = -W.\frac{\mu_{no}}{\sqrt{1+\left(\frac{\frac{C_{ox}.(V_{fbf}-V_{gs}+\phi_c(x))}{\varepsilon_{si}}}{E_c}\right)^2}}.2.(-C_{ox}.(V_{gs}+V_{sub}+\phi_F-V_{th}-\phi_c(x)).\frac{d\phi_c(x)}{dx}$$

$$=\frac{2.W.\mu_{no}.C_{ox}}{\sqrt{1+\left(\frac{C_{ox}}{\varepsilon_{si}.E_c}\right)^2(V_{fbf}-V_{gs}+\phi_c(x))^2}}.(V_{gs}+V_{sub}+\phi_F-V_{th}-\phi_c(x)).\frac{d\phi_c(x)}{dx} \tag{3.19}$$

Integrating equation (3.19) using boundary conditions (2.25) & (2.26)

$$\int_0^{L_g} I_{ds}\,dx=\int_{V_{bi}}^{V_{bi}+V_{ds}}\frac{2.W.\mu_{no}.C_{ox}.(V_{gs}+V_{sub}+\phi_F-V_{th}-\phi_c(x))}{\sqrt{1+\left(\frac{C_{ox}}{\varepsilon_{si}.E_c}\right)^2(V_{fbf}-V_{gs}+\phi_c(x))^2}}.d\phi_c(x) \tag{3.20}$$

Equation (3.20) can also be written as

$$\int_0^{L_1} I_1\,dx+\int_{L_1}^{L_g} I_2\,dx = \int_{V_{bi}}^{V_x}\frac{2.W.\mu_{no}.C_{ox}.(V_{gs}+V_{sub}+\phi_F-V_{th}-\phi_{c1}(x))}{\sqrt{1+\left(\frac{C_{ox}}{\varepsilon_{si}.E_c}\right)^2(V_{fbf1}-V_{gs}+\phi_{c1}(x))^2}}.d\phi_{c1}(x)\ +$$

$$\int_{V_x}^{V_{bi}+V_{ds}}\frac{2.W.\mu_{no}.C_{ox}.(V_{gs}+V_{sub}+\phi_F-V_{th}-\phi_{c2}(x))}{\sqrt{1+\left(\frac{C_{ox}}{\varepsilon_{si}.E_c}\right)^2(V_{fbf2}-V_{gs}+\phi_{c2}(x))^2}}.d\phi_{c2}(x)$$

$$=\int_0^{L_g} I_{ds}\,dx = I_{ds}.L_g \tag{3.21}$$

On solving for I_1 and I_2 separately, we get

$$I_{ds} = \frac{1}{L_g}\left[\begin{array}{l}\left\{\frac{2.W.\mu_{no}.C_{ox}}{(d_3)^{\frac{3}{2}}}\times(1+A_1)\times\left[(d_2+d_4).\ln\left(\frac{c_1+c_2}{c_{11}+c_{22}}\right)-c_2+c_{22}\right]\right\} \\ +\left\{\frac{2.W.\mu_{no}.C_{ox}}{(d_3)^{\frac{3}{2}}}\times(1+A_1)\times\left[(d_2+d'_4).\ln\left(\frac{c'_1+c'_2}{c'_{11}+c'_{22}}\right)-c'_2+c'_{22}\right]\right\}\end{array}\right] \tag{3.22}$$

where $d_2 = V_{gs} - V_{th} + \phi_F$, $d_3 = \left(\frac{C_{ox}}{\varepsilon_{si}.E_c}\right)^2$, $d_4 = V_{fbf1} - V_{gs}$, $A_1 = \frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{ox}}$

$c_1 = [d_3.d_4 + d_3.(V_x)]$, $c_2 = \sqrt{1+d_3.(d_4)^2 + 2.d_3.d_4.(V_x) + d_3.(V_x)^2}\times\sqrt{d_3}$, $d'_4 = V_{fbf2} - V_{gs}$

$c_{11} = [d_3.d_4 + d_3.(V_{bi})], c_{22} = \sqrt{1+d_3.(d_4)^2 + 2.d_3.d_4.(V_{bi}) + d_3.(V_{bi})^2}\times\sqrt{d_3}$,

$c'_{11} = [d_3.d'_4 + d_3.(V_x)], c'_{22} = \sqrt{1+d_3.(d'_4)^2 + 2.d_3.d'_4.(V_x) + d_3.(V_x)^2}\times\sqrt{d_3}$,

$c'_1 = [d_3.d'_4 + d_3.(V_{bi})]\ c'_2 = \sqrt{1+d_3.(d'_4)^2 + 2.d_3.d'_4.(V_{bi}+V_{ds}) + d_3.(V_{bi}+V_{ds})^2}\times\sqrt{d_3}$

here V_x is calculated using $\int_{V_{bi}}^{V_x} I_{ds1}(L_1,0)\,dx = \int_{V_x}^{V_{bi}+V_{DS}} I_{ds2}(L_1,0)\,dx$, which is the condition of continuity of current in the channel at the boundary of M1 and M2. The above expression for drain-current is valid for linear region only. For saturation region, same equation 3.22 is used by replacing the normal channel length, L_g with reduced channel length $(L_g - l_d)$ and V_{ds} with V_{dsat} (derived in equation 3.25). Here, l_d is the distance by which channel length is shortened when V_{ds} increases beyond $V_{dsat,}$ given by

$$l_d = \sqrt{\frac{2.\varepsilon_o.\varepsilon_{si}}{q.N_a(y)}(V_{ds} - V_{dsat})} \tag{3.22a}$$

The term $(1+A_1)$ relates $\phi_s(x)$ and $\phi_c(x)$ (from equation (2.36)) as given below

$$\frac{d\phi_c(x)}{dx} = (1+A_1).\frac{d\phi_s(x)}{dx} \tag{3.23}$$

As the carriers at the drain end are velocity saturated, the saturated drain-source current is given by

$$I_{Dsat} = -2.W.v_{sat}.Q_{sat}(x) = 2.W.v_{sat}.C_{ox}(V_{gs} + V_{sub} - V_{th} + \phi_F - \phi(x)) \qquad (3.24)$$

where $Q_{sat}(x)$ is the value of $Q_n(x)$ at $\phi(x) = V_{dsat}$, v_{sat} is the saturation velocity. Taking $v_{sat} = \frac{E_c}{\mu_s}$, $n=1$ in $\left(1+\left(\frac{E(x)}{E_c}\right)^n\right)^{\frac{1}{n}}$, $E(x) = \frac{d\phi(x)}{dx}$ in equation (3.19) and by equating equation (3.24) and equation (3.19), we can calculate V_{dsat}. The resulting quadratic equation gives V_{dsat}, which is written as

$$V_{dsat} = \frac{1}{2.\alpha.\mu_s}\left(4.V_{th}.\mu_s - 2.\alpha.L_g.v_{sat} + 2.\sqrt{4.V_{th}^2.\mu_s^2 + \alpha^2.L_g^2.v_{sat}^2 + 2.\mu_s.\alpha.L_g.v_{sat}.(V_{gs} - V_{th})}\right) \qquad (3.25)$$

Figure 3.11 shows the variation of drain-current (as calculated using equation 3.22) with drain-source voltage for different gate-source voltages for *DM DG* structure and *SM DG* structure. It is seen that the drain current in general increases when the gate metal work function is higher. It is also observed that for smaller gate to source voltage, drain current is more or less same for both the structures.

In figure 3.12, the drain current has been plotted for gate to source voltage for a fixed value of V_{ds}. It is another method to calculate threshold voltage.

In figure 3.13, I_{ds} vs V_{ds} characteristics as computed using the analytical model and using device simulator *ATLAS* are shown. A close agreement between the two characteristic is observed.

In figure 3.14, the saturation drain voltage has been plotted against gate to source voltage for different values of channel length L_g. It is observed that saturation drain voltage is larger for large channel length for given gate to source voltages, as expected.

Figure 3.15 shows the drain current vs drain voltage characteristics for different doping distribution. It is seen that drain current is more in case of Pearson-IV distribution in comparison to other cases indicating that *DM DG* structure with Pearson-IV distribution allows for higher current capability.

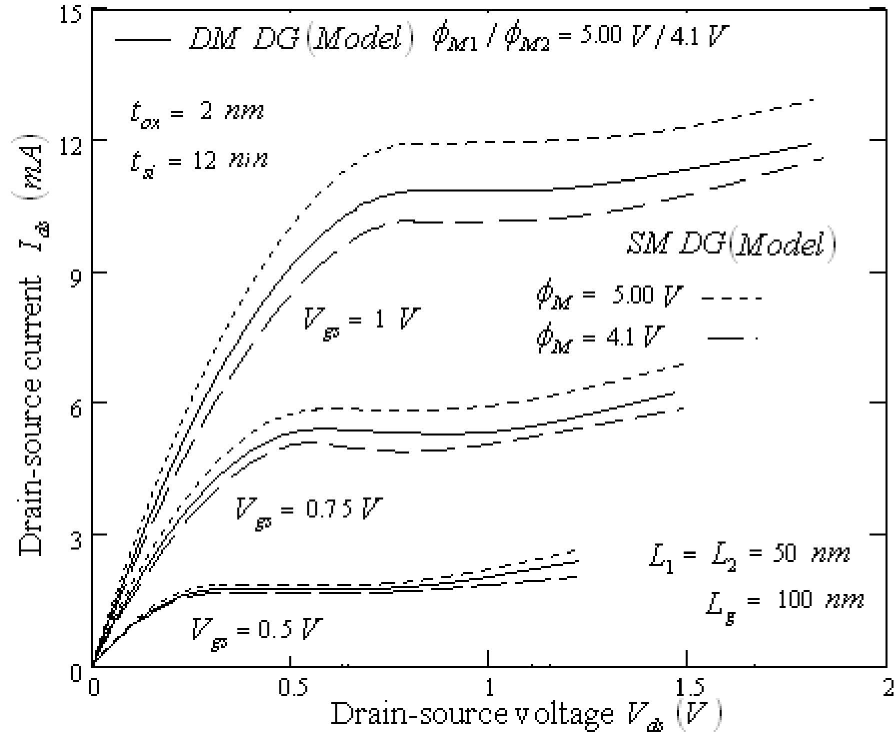

Fig 3.11 Drain-source current vs drain-source voltage for different gate-source voltages in DM DG and SM DG SOI structures.

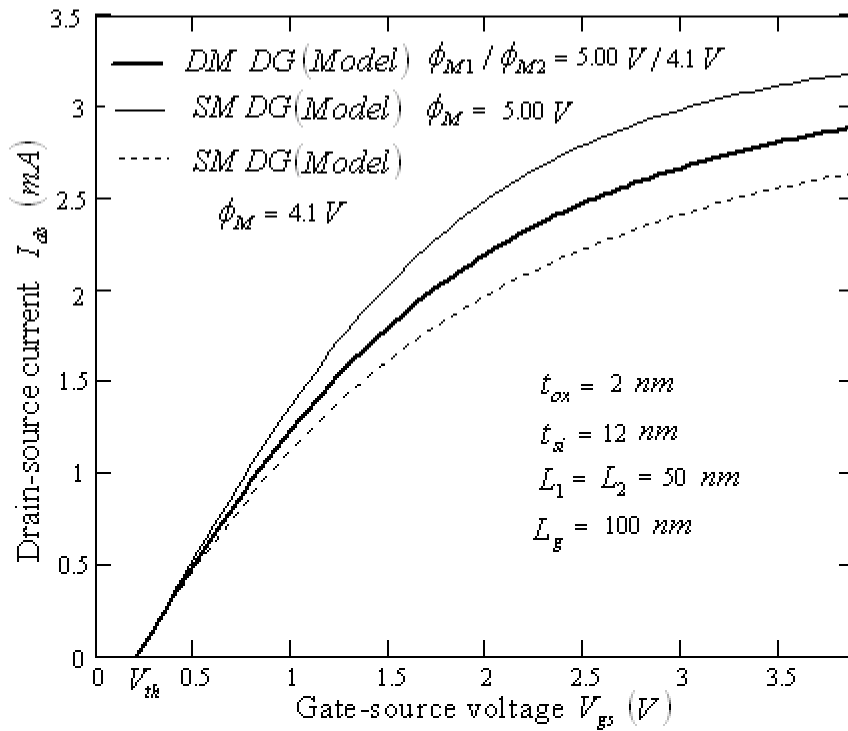

Fig 3.12 Drain-source current vs gate-source voltage for V_{ds}= 50 mV in DM DG and SM DG SOI structures.

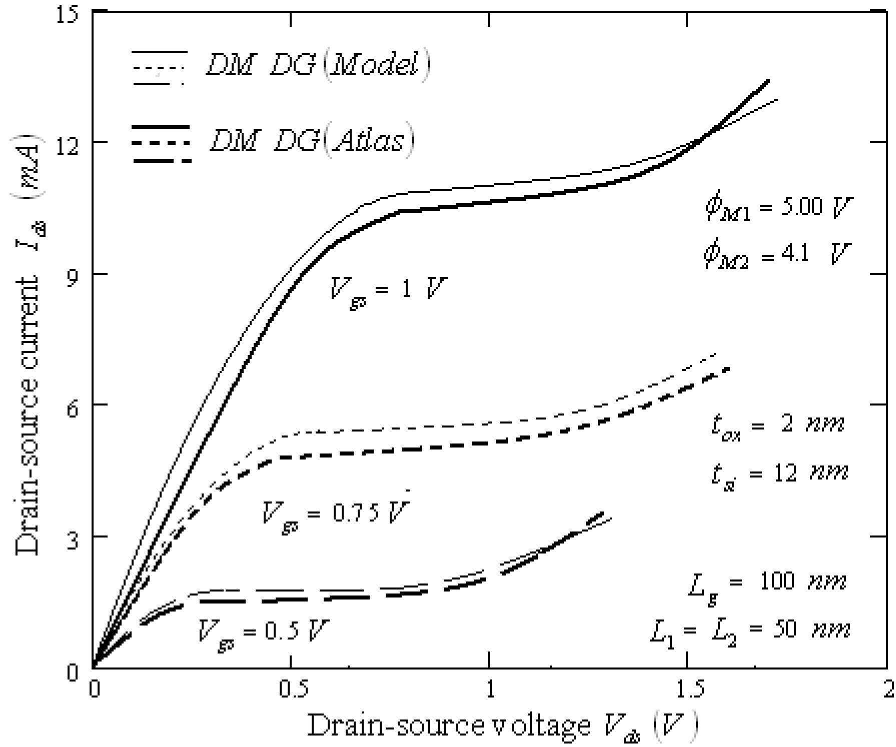

Fig 3.13 Drain-source current vs drain-source voltage for different gate-source voltage in DM DG and SM DG SOI structures.

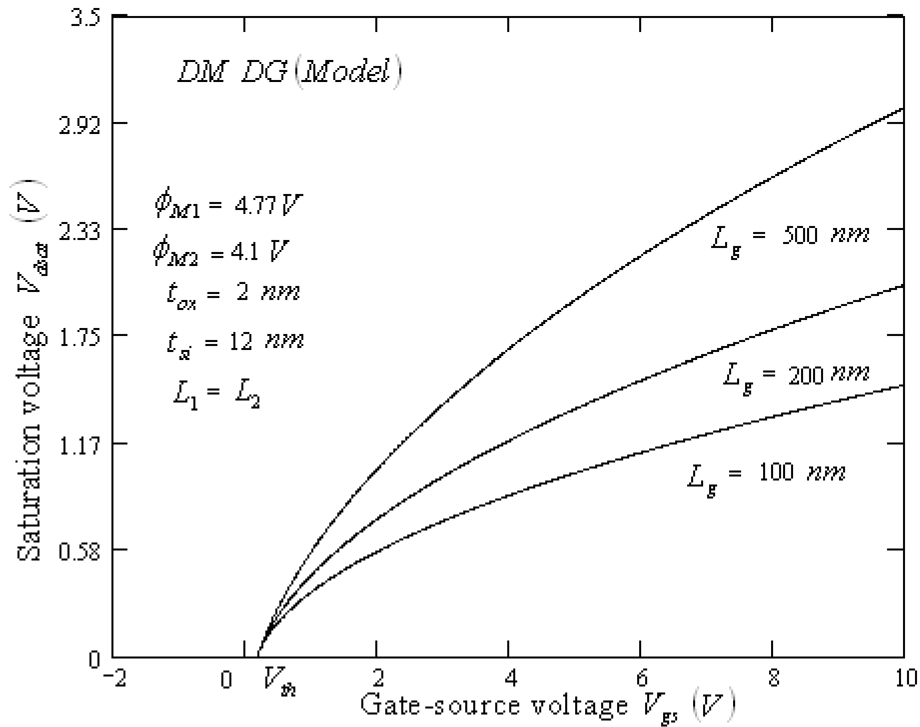

Fig 3.14 Saturation voltage vs gate-source voltage for different gate length in DM DG SOI structure.

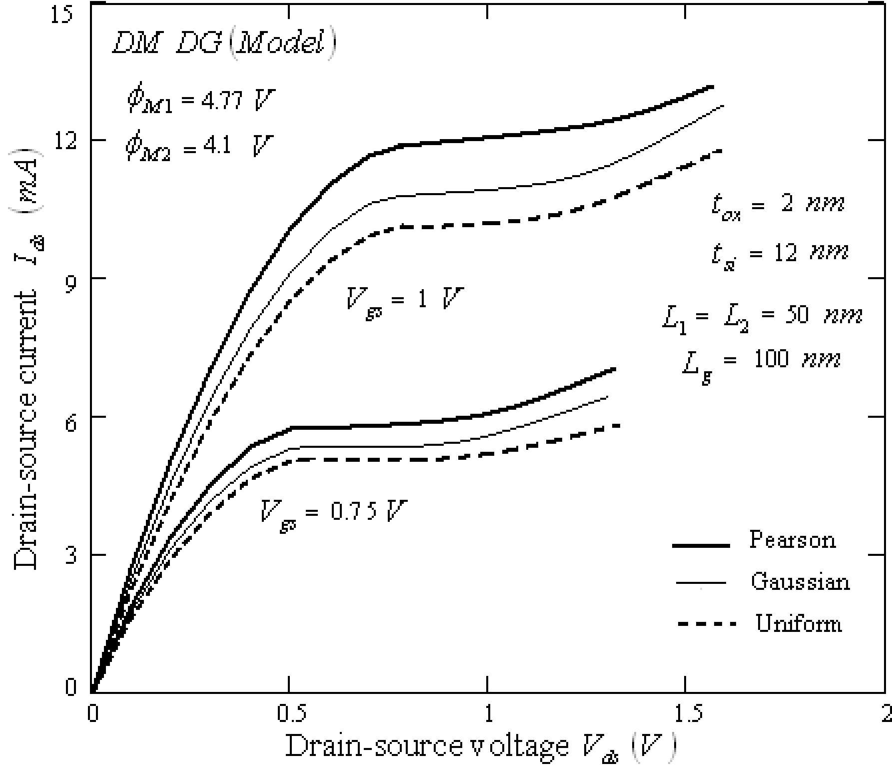

Fig 3.15 Drain-source current vs drain-source voltage characteristics in DM DG structure with different distribution functions.

3.5 Transconductance

The transconductance of the *n*-channel *DM DG FD SOI MOSFET* is obtained by differentiating the drain-current with respect to gate-source voltage for a constant drain to source voltage and is expressed as

$$g_m = \left(\frac{dI_{ds}}{dV_{gs}}\right)\Bigg|_{V_{ds}=const.} \tag{3.26}$$

Using equation (3.22) the expression for g_m is derived as given below

$$g_m = \frac{2.W.\mu_{no}.C_{ox}}{L_1.(d_3)^{\frac{3}{2}}}\times(1+A_1)\times\left[(d_2+d_4).(c_{111})+\left(\frac{c_1}{c_2}-\frac{c_{11}}{c_{22}}\right).\sqrt{d_3}\right] + \frac{2.W.\mu_{no}.C_{ox}}{L_2.(d_3)^{\frac{3}{2}}}\times(1+A_1)\times\left[(d_2+d'_4).(c_{222})+\left(\frac{c'_1}{c'_2}-\frac{c'_{11}}{c'_{22}}\right).\sqrt{d_3}\right] \tag{3.27}$$

$$\text{where } c_{111} = \frac{\left(d_3 + \frac{\sqrt{d_3}.c_{11}}{c_{22}}\right).d_3}{c_{11} + c_{22}.\sqrt{d_3}} - \frac{\left(d_3 + \frac{\sqrt{d_3}.c_1}{c_2}\right).d_3}{c_1 + c_2.\sqrt{d_3}} \qquad \text{and}$$

$$c_{222} = \frac{\left(d_3 + \frac{\sqrt{d_3}.c'_{11}}{c'_{22}}\right).d_3}{c'_{11} + c'_{22}.\sqrt{d_3}} - \frac{\left(d_3 + \frac{\sqrt{d_3}.c'_1}{c'_2}\right).d_3}{c'_1 + c'_2.\sqrt{d_3}};$$

where $d_2, d_3, d_4, d'_4, c_1, c_2, c_{11}, c_{22}, c'_1, c'_2, c'_{11}$ and c'_{22} are as defined for equation 3.22. Figure 3.16 and 3.17 show the transconductance vs gate-source voltage characteristics for *DM DG* and *SM DG SOI* structures. It is seen that transconductance is significantly larger in case of *DM DG SOI* structure indicating that the gate has better control over the conductance in case *DM DG SOI* structure.

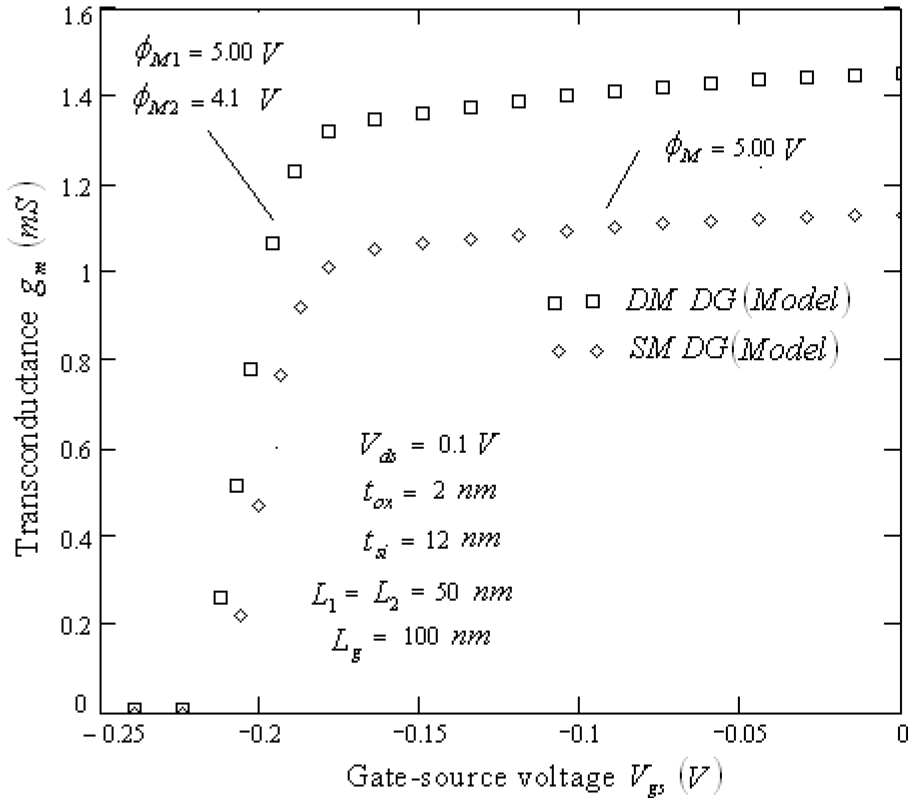

Fig 3.16 Transconductance vs gate-source voltage in DM DG and SM DG SOI structures for –ve gate to source voltage.

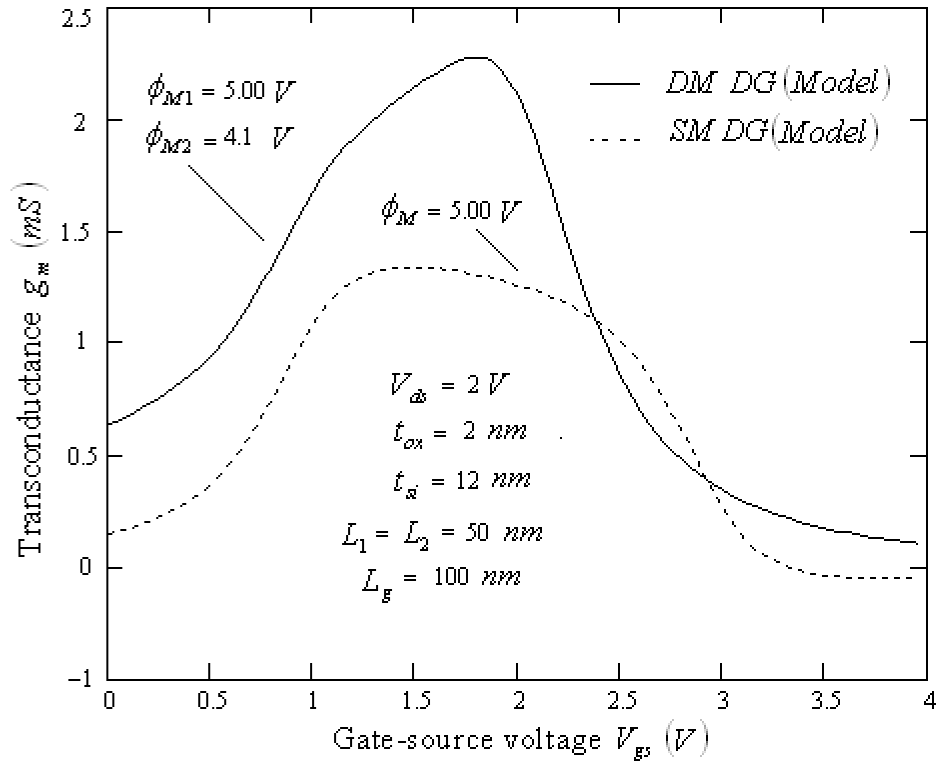

Fig 3.17 Transconductance vs gate-source voltage in DM DG and SM DG SOI structures for +ve gate to source voltage.

Figure 3.18 shows the transconductance vs gate-source voltage characteristics for different combinations of work functions of M1 and M2. It is observed that larger the work functions difference larger is transconductance.

Figure 3.19 shows the comparison between transconductance vs gate-source voltage characteristics as computed using analytical model and device simulator *ATLAS*. The two are observed to be in close agreement.

Figure 3.20 shows the transconductance vs gate-source voltage characteristics for different values of channel lengths *i.e. 100 nm, 200 nm, 500 nm*. As expected, transconductance decreases with increasing channel length.

Figure 3.21 shows the transconductance vs gate-source voltage characteristics for different doping distribution. It is observed that in case of Pearson IV distribution the transconductance is significantly larger as compared to the same in other cases.

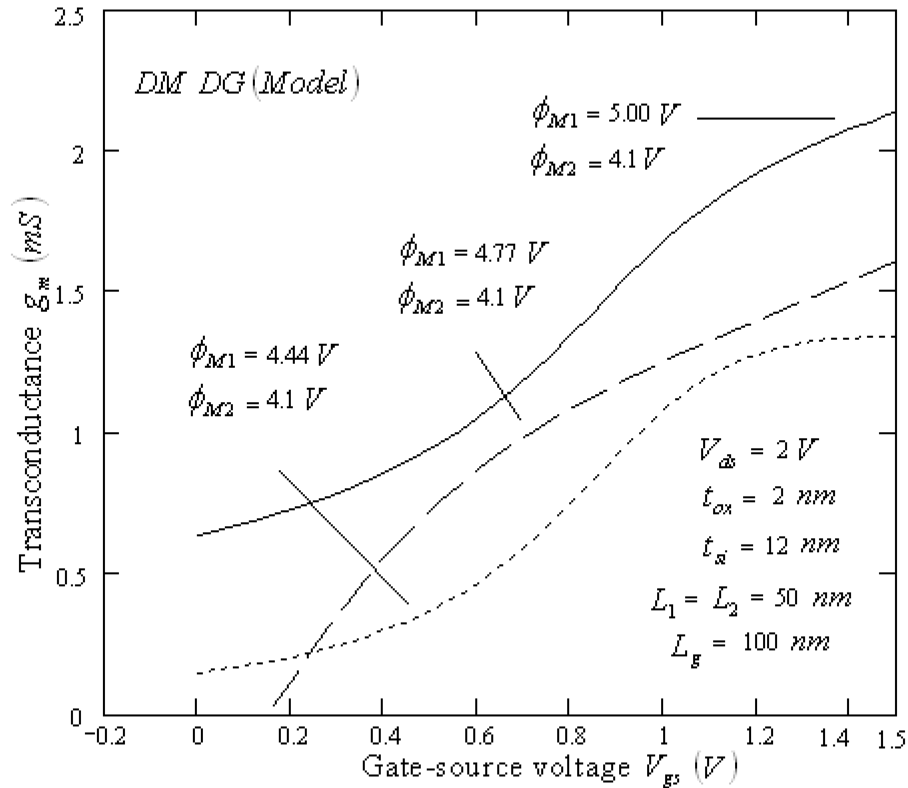

Fig 3.18 Transconductance vs gate-source voltage on different combinations of work function in DM DG SOI structure.

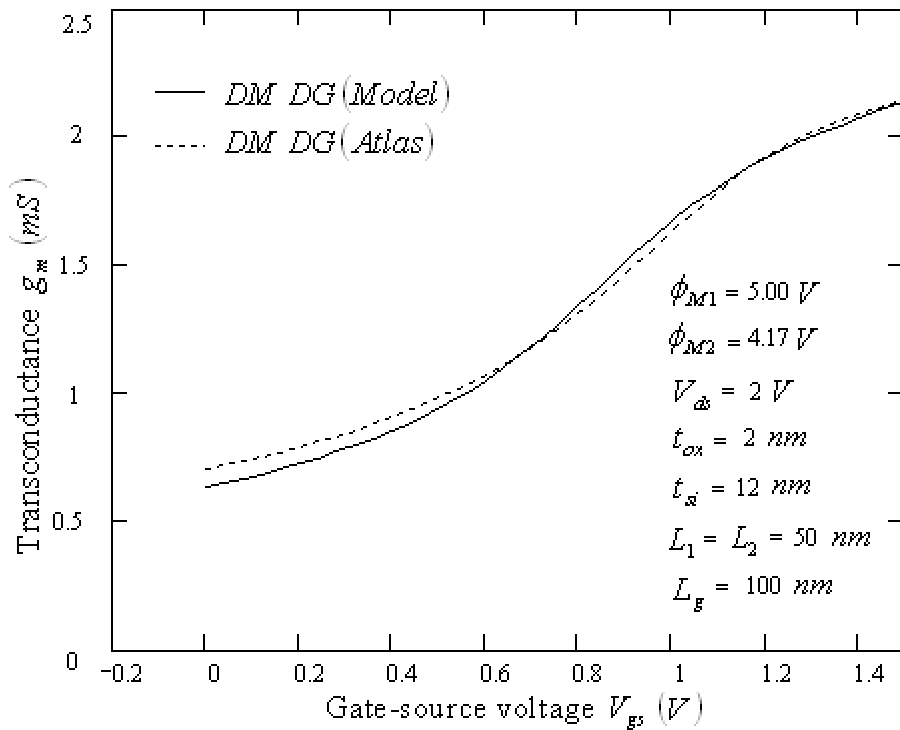

Fig 3.19 Comparison between analytical model and device simulator values for transconductance in DM DG SOI structure.

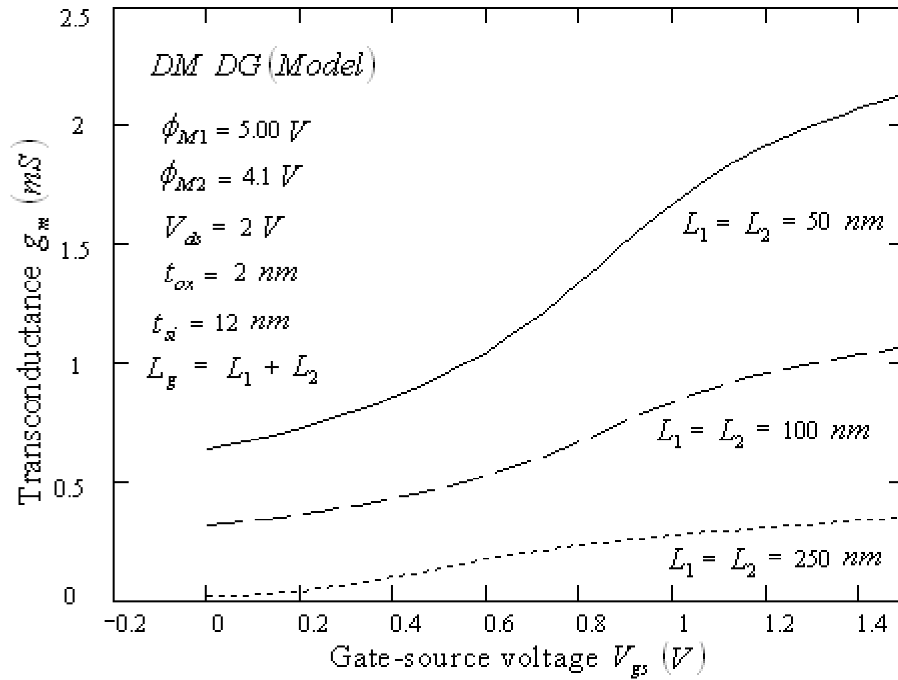

Fig 3.20 Transconductance vs gate-source voltage for different combinations of L_1 and L_2 in DM DG SOI structure.

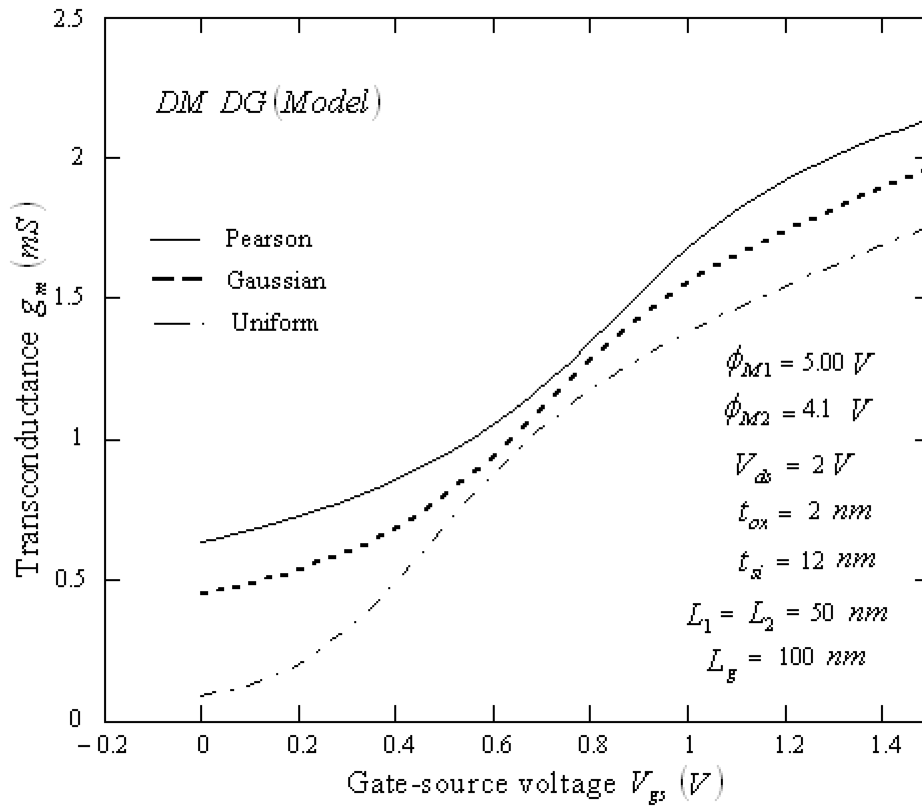

Fig 3.21 Transconductance vs gate-source voltage for different doping distribution in DM DG structure**.**

3.6 Drain Resistance

Drain resistance (r_{ds}) is important for design of high frequency, low-voltage devices. It can be expressed as

$$r_{ds} = \left(\frac{dI_{ds}}{dV_{ds}}\right)^{-1}\Bigg|_{V_{gs}=const.} \tag{3.28}$$

Using equation 3.22, the expression for r_{ds} is derived to be,

$$r_{ds} = \frac{2.W.\mu_{no}.C_{ox}}{L_1.(d_3)^{\frac{3}{2}}}\times(1+A_1)\times\left[(d_2+d_4).(c'_{111})-\left(\frac{c_1}{2.c_2}\right).\sqrt{d_3}\right] + \frac{2.W.\mu_{no}.C_{ox}}{L_{2.}(d_3)^{\frac{3}{2}}}\times(1+A_1)\times\left[(d_2+d'_4).(c'_{222})+\left(\frac{c'_{11}}{2.c'_{22}}-\frac{c'_1}{2.c'_2}\right).\sqrt{d_3}\right] \tag{3.29}$$

where $c'_{111} = \dfrac{\left(\dfrac{d_3}{2}+\dfrac{\sqrt{d_3}.c_1}{c_2}\right).d_3}{c_1+c_2.\sqrt{d_3}}$, $c'_{222} = \dfrac{\left(\dfrac{d_3}{2}+\dfrac{\sqrt{d_3}.c'_1}{2.c'_2}\right).d_3}{c'_1+c'_2.\sqrt{d_3}} - \dfrac{\left(\dfrac{d_3}{2}+\dfrac{\sqrt{d_3}.c'_{11}}{2.c'_{22}}\right).d_3}{c'_{11}+c'_{22}.\sqrt{d_3}}$

All others constants $d_2, d_3, d_4, d'_4, c_1, c_2, c_{11}, c_{22}, c'_1, c'_2, c'_{11}$ and c'_{22} are as defined for equation (3.22).

In figure 3.22 the drain-resistance has been plotted against drain-source voltage for *DM DG* and *SM DG SOI* structures as computed using equation (2.29). It is observed that the drain-resistance in case of *DM DG SOI* structure is lower than that of *SM DG SOI* structure. This is consistent with higher current drive capability of the *DM DG SOI* structure.

Figure 3.23 shows the drain resistance vs drain-voltage characteristics for different combinations of work functions of M1 and M2. It is observed that as the work functions difference decreases the drain-resistance increases.

In figure 3.24, the drain-resistance vs drain voltage characteristics has been plotted, as computed from equation (3.29) and using device simulator *ATLAS*. The two characteristics are in very close agreement indicating the high accuracy of the analytical model.

Figure 3.25 shows the drain resistance vs drain-voltage characteristics for different gate lengths *i.e. 100 nm, 200 nm, 500 nm*. As expected the drain resistance increases with increasing channel length.

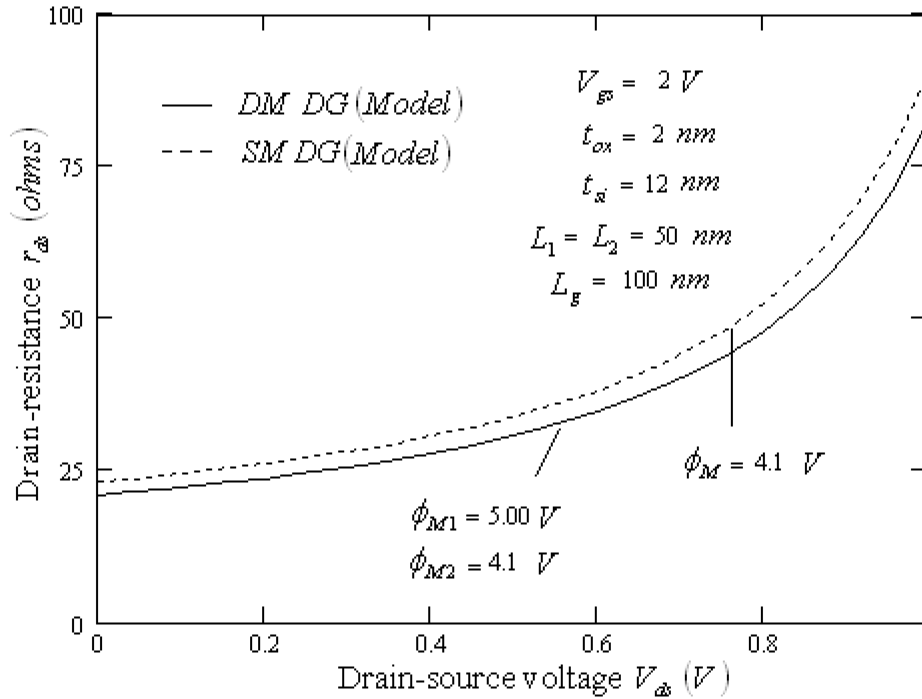

Fig 3.22 Drain-resistance vs drain-source voltage in DM DG and SM DG SOI structures.

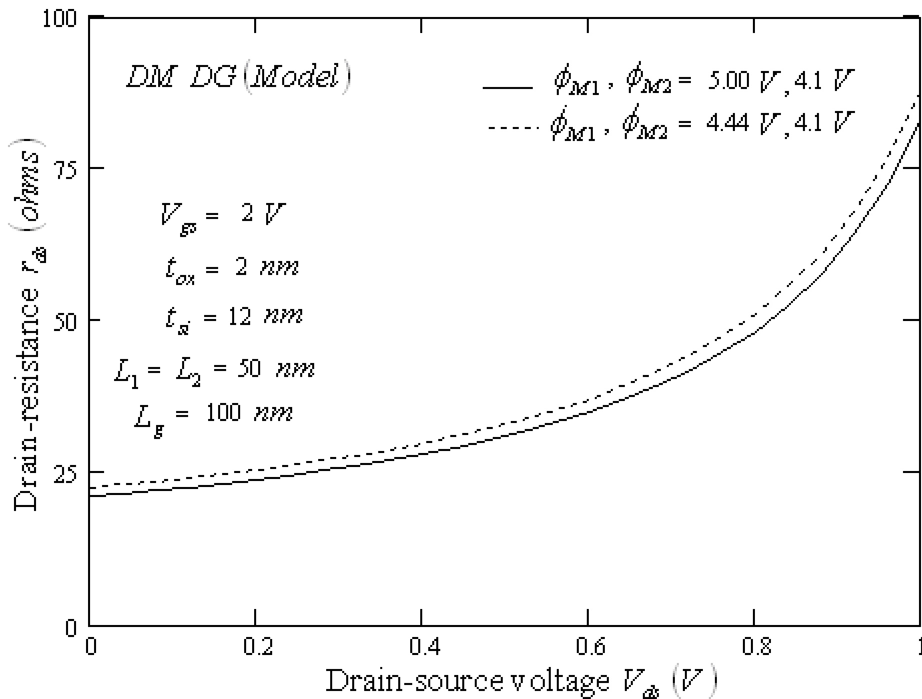

Fig 3.23 Drain-resistance vs drain-source voltage for different work functions for DM DG SOI structure.

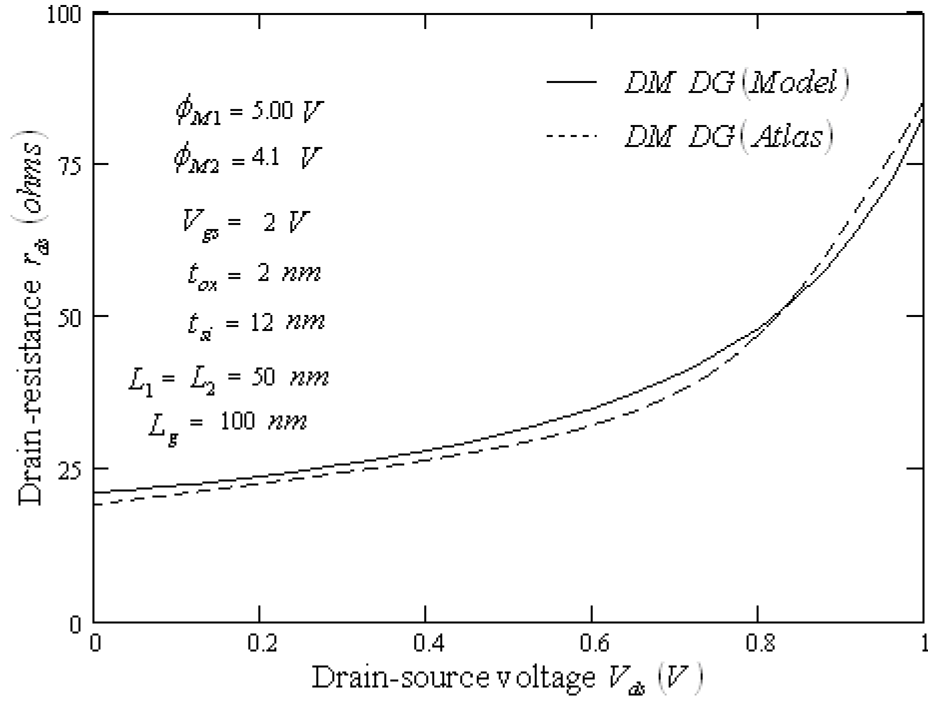

Fig 3.24 Comparison between analytical model and device simulator values for drain resistance in DM DG SOI structure.

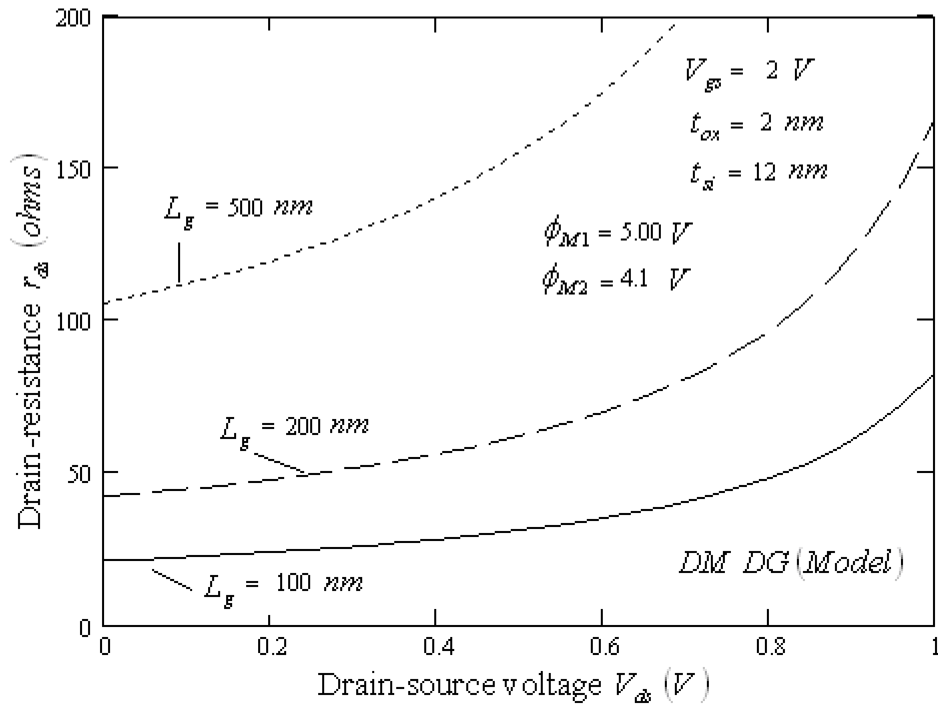

Fig 3.25 Drain-resistance vs drain-source voltage for different combinations of L_1 and L_2 in DM DG SOI structure.

Figure 3.26 shows the plot of drain-resistance vs drain-voltage for different doping distribution. It is seen that the drain resistance is lowest in case of Pearson IV doping distribution.

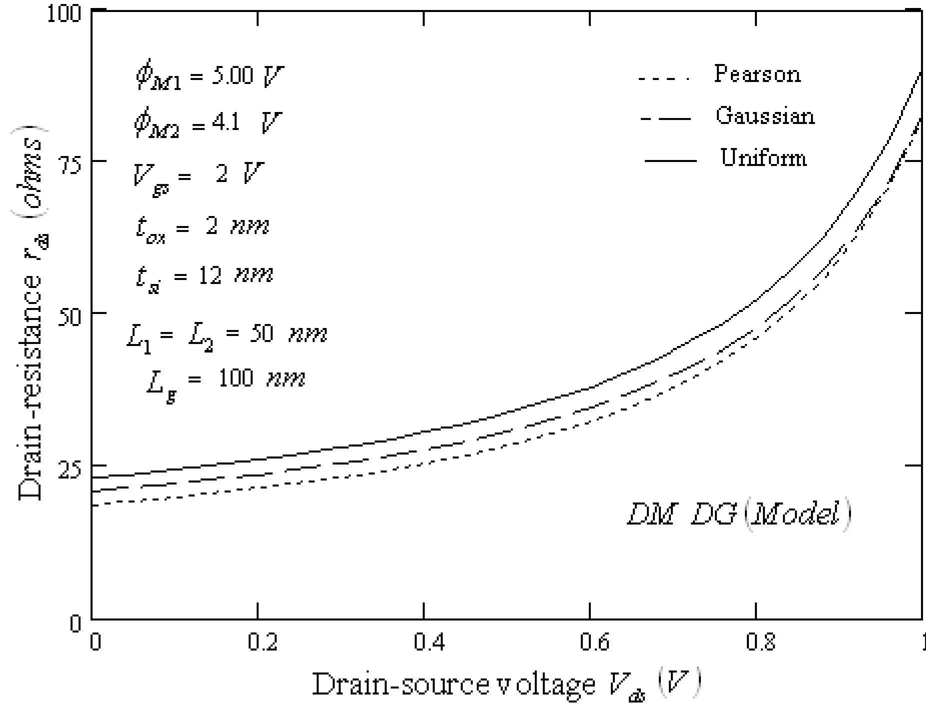

Fig 3.26 Drain-resistance vs drain-source voltage for different doping distribution in DM DG structure.

3.7 Cut-off Frequency

The cut-off frequency is one of the important figure of merit of low-voltage and high-speed devices. The cut-off frequency increases as the size of the device decreases. It is expressed as

$$f_c = \frac{g_m}{2.\pi.L_g.C_T} \tag{3.30}$$

where g_m is the transconductance of the device, L_g is the channel-length (equal to $L_1 + L_2$) and C_T is the total device capacitance. Figure 3.27 shows the plot of cut-off frequency vs channel-length for a given gate-source voltage for *DM DG FD SOI MOSFETs* as computed from the analytical model (i.e. analytical equation developed in chapter 2 & 3). It is seen that the cut-off frequency decreases as the gate to source voltage

increases which is because of lower value of transconductance on higher gate to source voltage.

Figure 3.28 shows a comparison between cut off frequency for *DM DG* and *SM DG* structures as computed using analytical model. It is seen that the *DM DG* structure offers higher cutoff frequency which is because of higher transconductance of *DM DG* structure.

Figure 3.29 shows the plot of cut off frequency vs channel length for *DM DG* structure as computed using analytical model and using device simulator *ATLAS*. The two curves are in very good agreement bringing out the correctness of the proposed analytical model. Figure 3.30(a) shows the variation of the cut-off frequency with gate-source voltage for different channel lengths *i.e. 100 nm, 250 nm, 500 nm,* as computed using analytical model. As expected that the cut-off frequency decreases with increasing channel length. Figure 3.30(b) shows the variation of the cut-off frequency along the channel length for different values of V_{ds} for DM DG structure. It is increasing with increasing value of V_{ds} as transconductance is increasing.

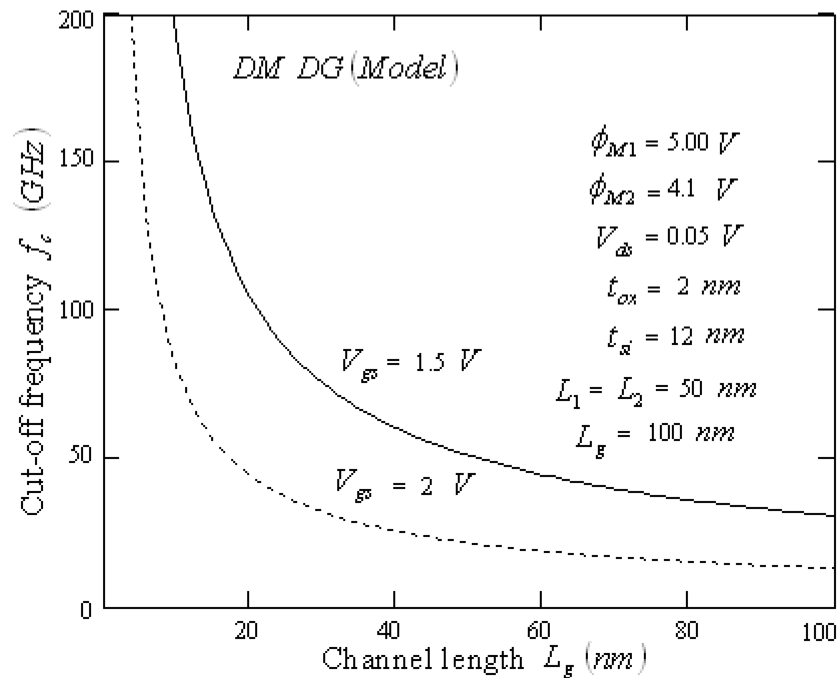

Fig 3.27 Variation of cut-off frequency along the channel-length for different gate-source voltages in DM DG SOI structure.

3.8 Transit time

The carrier transit time through the channel is the measure of the speed of the device. There are two constraints which limit the speed of the device. First constraint is the time for charge transport along the channel. Second constraint is the charging time constant for the device capacitance. The transit time of a *MOSFET* is the inverse of the cut-off frequency, written as

$$\tau = \frac{1}{f_c} \tag{3.31}$$

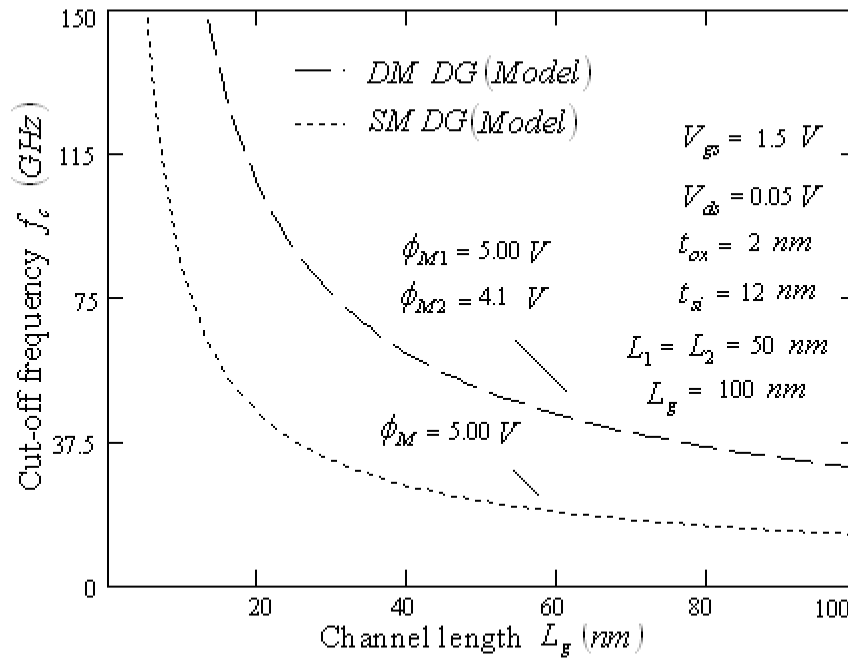

Fig 3.28 Variation of cut-off frequency along the channel-length in DM DG and SM DG SOI structures.

Figure 3.31 shows the variation of transit time with channel length for different gate-source voltages (computed using analytical model). It is observed that transit time increases with increase in channel length. Figure 3.32 shows the plot of transit time against channel length for different oxide thickness. As expected the larger oxide thickness leads to smaller capacitance, higher cut off frequency and therefore, smaller transit time.

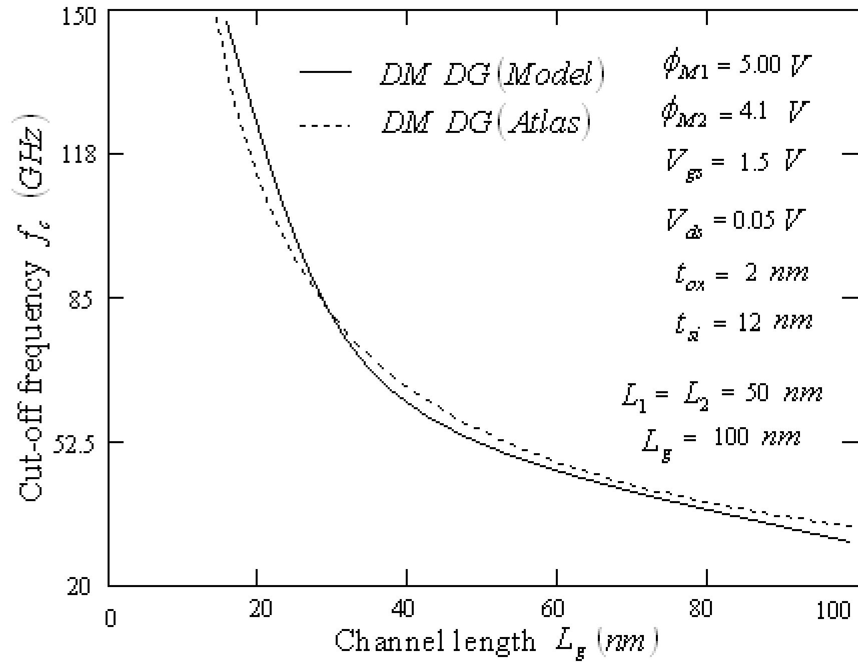

Fig 3.29 Comparison between analytical model and device simulator values for cut-off frequency along the channel length in DM DG SOI structure.

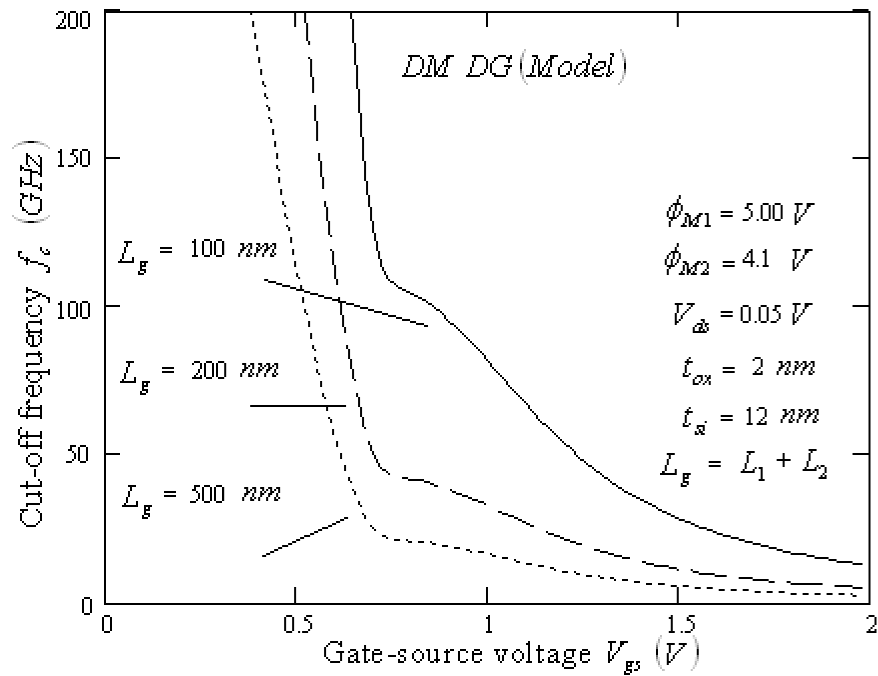

Fig 3.30 (a) Cut-off frequency vs gate-source voltage for different combinations of L_1 and L_2 in DM DG SOI structure.

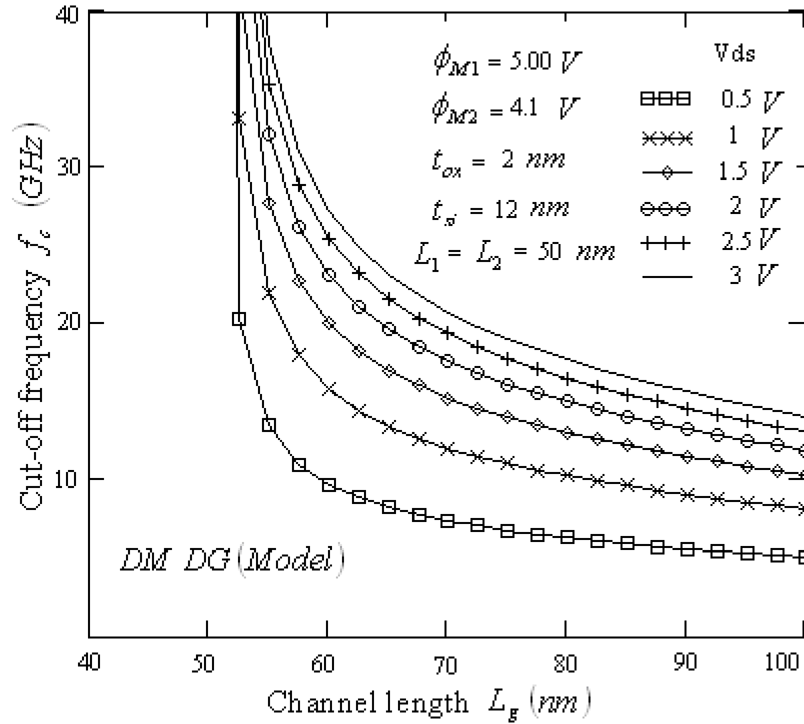

Fig 3.30 (b) Variation of cut-off frequency along the channel-length for different drain-source voltages in DM DG SOI structure.

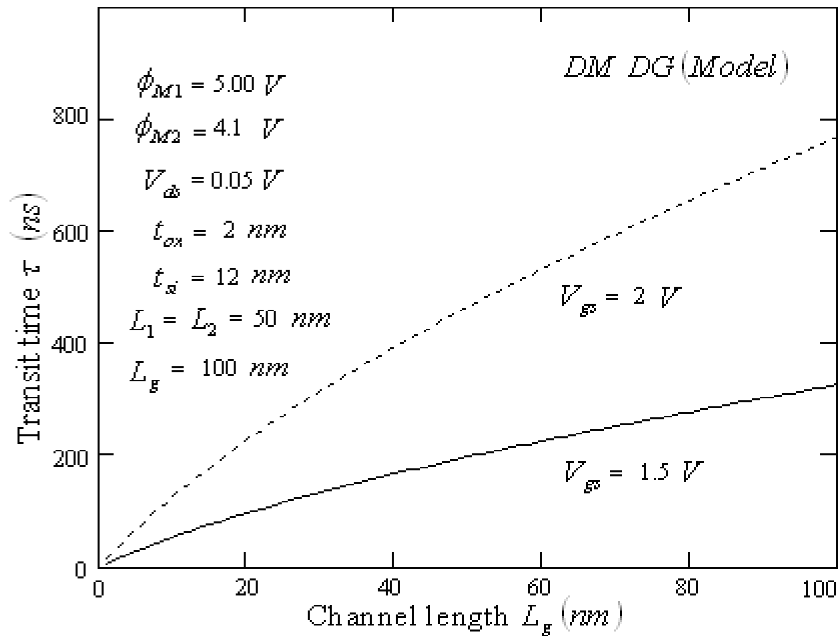

Fig 3.31 Variation of transit time along the channel length for different gate-source voltage in DM DG SOI structure.

3.9 Noise

It has so far been assumed that the drain-source current of a *MOS* transistor varies with time only if one or more of the terminal voltages vary with time. This is not exactly true. A careful examination of the current reveals minute fluctuations, referred to as noise. For optimized circuit design accurate noise characterization is essential [97]-[99]. The thermal noise and flicker noise which are most important for *DM DG SOI MOSFET* have been considered in the following subsections.

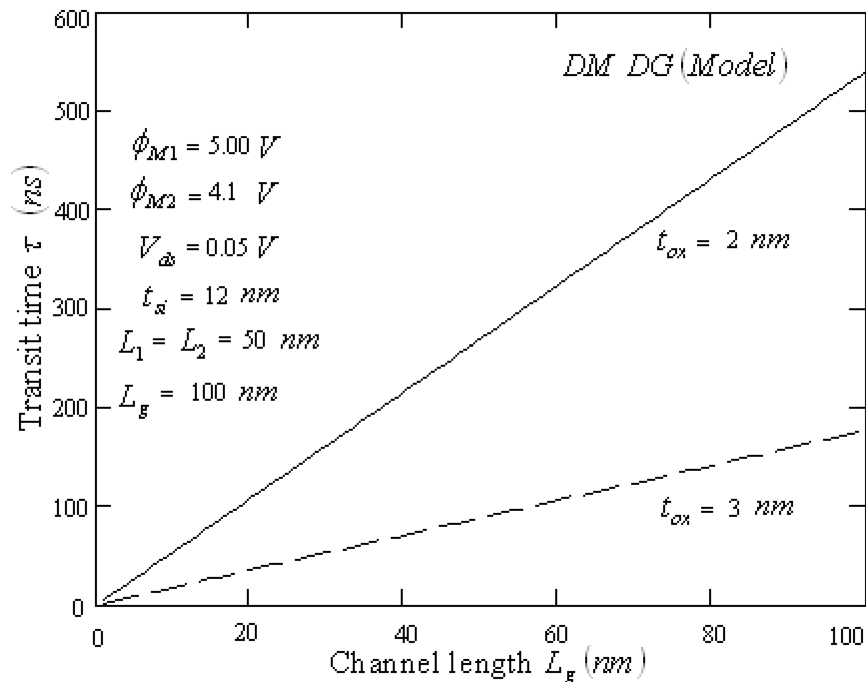

Fig 3.32 Variation of transit time along the channel length for different oxide layer thickness in DM DG SOI structure.

3.9.1 Thermal Noise

The expression thermal noise [100] is given by

$$S_{vt} = 4.k.T.R \tag{3.32}$$

where k is Boltzmann's constant, T is absolute temperature, S_{vt} is the Noise Power Spectral density and R is the drain resistance given by equation (3.28). Figure 3.33 shows the plot of thermal noise power spectral density vs drain-source voltage for different temperatures for *DM DG* and *SM DG SOI* structures. In the

expression 3.32, *R* has been taken to be drain resistance as given by equation (3.28). It is seen that the noise power spectral density increases as the temperature increases and also for *DM DG SOI* structure, the noise power spectral density is smaller as compared to the same for *SM DG* structure.

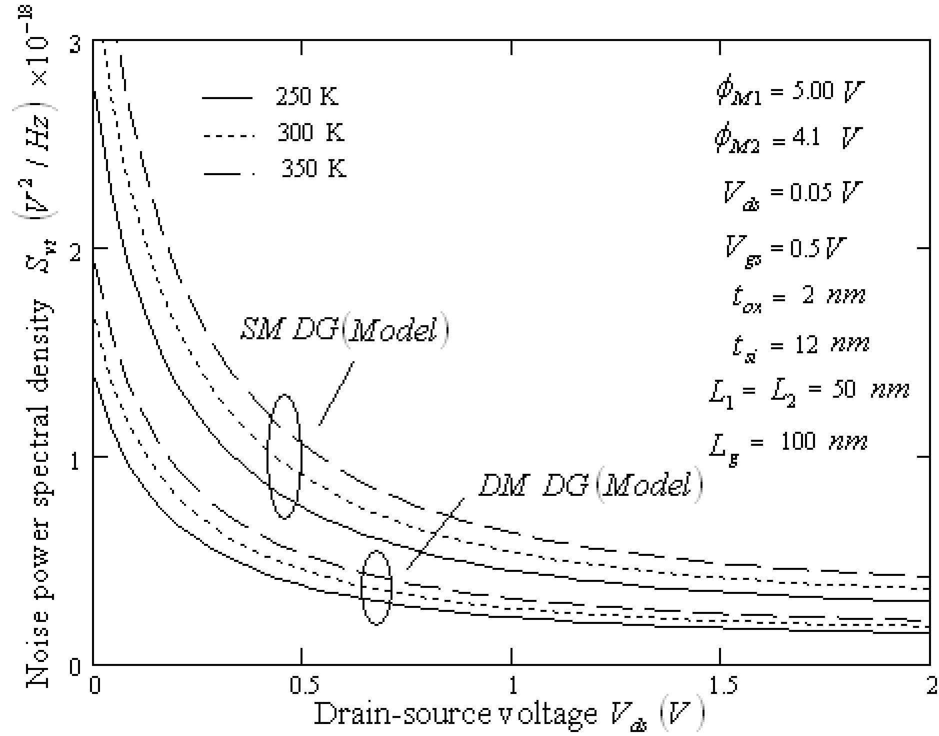

Fig 3.33 Variation of Noise Power Spectral Density along the drain-source voltage for different temperatures in SM DG and DM DG SOI structures.

3.9.2 Flicker Noise

Flicker noise in *MOS* transistors has been the subject of intense studies for several decades. There are several theories for the origin of this noise, which involved sometimes conflicting conclusions and several issues remaining unresolved [97], [101]-[111]. The first theory attributes the origin of flicker noise to the random fluctuation of the density of carriers in the channel due to fluctuations in the surface potentials. These fluctuations are in turn caused by trapping and releasing of carriers by traps located near the $Si\text{-}SiO_2$ interface [112]-[113]. It has been shown that a power spectral density nearly proportional to the inverse of the frequency results [97], [114].

A second theory attributes flicker noise to mobility fluctuations, due to carriers' interactions with lattice fluctuations [115]-[118]. Some research suggests that flicker noise is due to both carrier number fluctuations and mobility fluctuations [119].
Using detailed physical consideration, the power spectral density of the equivalent flicker noise voltage has shown to be [112],[120].

$$S_{vf}(f) = \frac{K_1}{C_{ox}^2 W L_g f^c} \tag{3.33}$$

where, for *n*-channel devices, the exponent c varies between 0.7 and 1.2 and K_1 is a quantity independent of bias but depends on fabrication processes, usually K_1 varies between 5×10^{-31} - $1\times10^{-30} C^2/cm^2$. Figure 3.34 shows the plot of noise power spectral density and cut-off frequency for *DM DG* and *SM DG SOI* structures for $c = 0.8$. Figure 3.35 shows a plot similar to that in figure 3.34 with $c = 1.2$. Corresponding to this noise power spectral density of equivalent drain noise current can be shown as

$$S_{if}(f) = g_m^2 S_{vf}(f) \tag{3.34}$$

On the basis of second theory, flicker noise due to lattice vibration (due to carrier interaction with lattice fluctuations), the power spectral density for the equivalent noise voltage is

$$S_{vf}(f) = \frac{K(V_{gs})}{C_{ox} W L_g f} \tag{3.35}$$

where $K(V_{gs})$ is a bias dependent quantity and is of the order of 6×10^{-26} to $2\times10^{-23} V^2 F$.

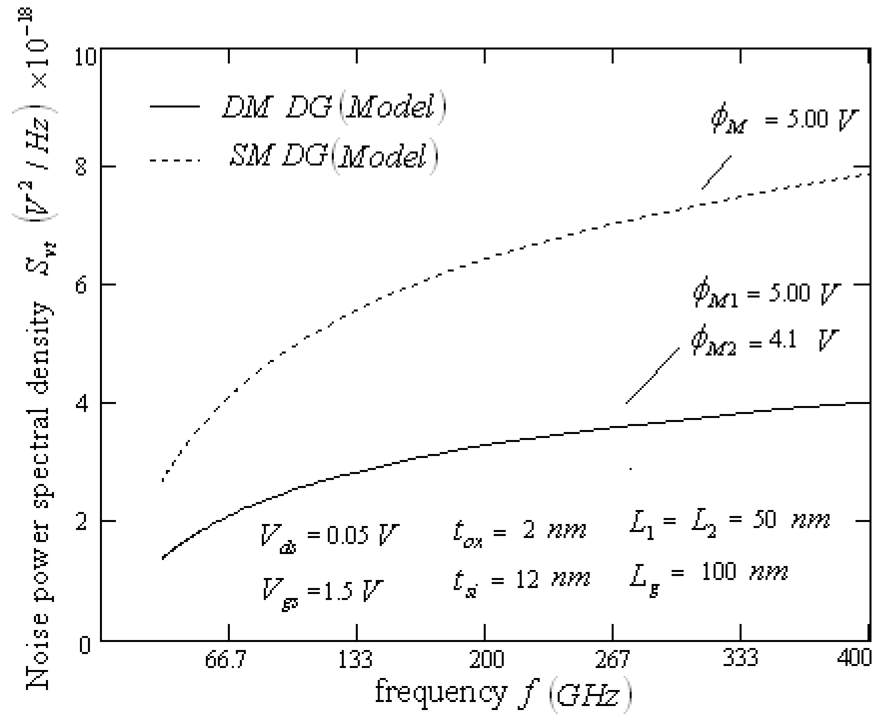

Fig 3.34 Variation of Noise Power Spectral Density along the cut-off frequency for c = 0.8 in SM DG and DM DG SOI structures.

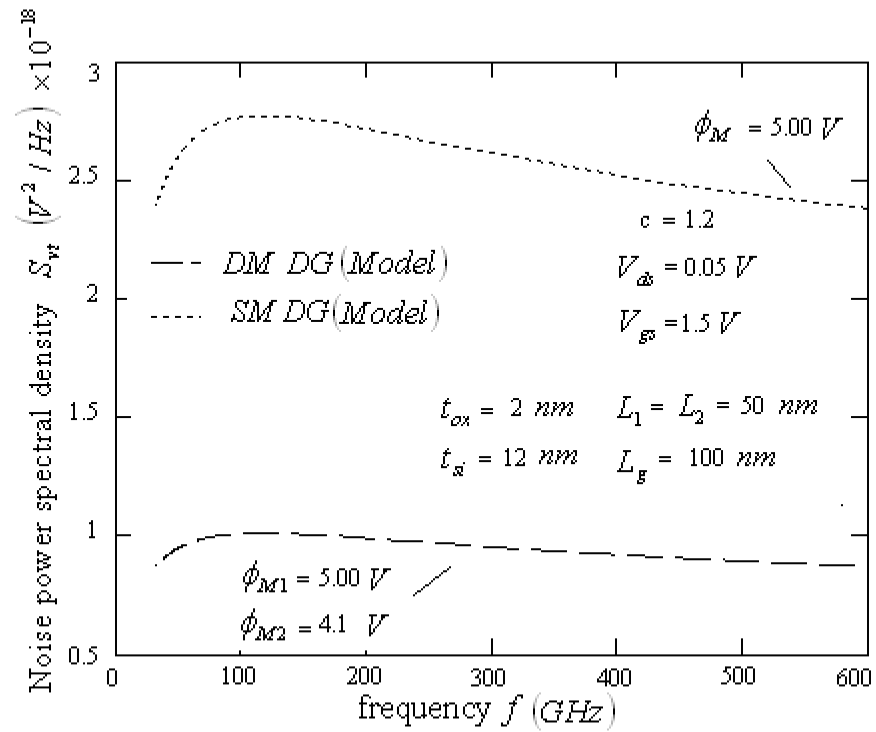

Fig 3.35 Variation of Noise Power Spectral Density along the cut-off frequency for c =1.2 in SM DG and DM DG SOI structures.

3.10 Summary

In this chapter the closed form equations have been developed for the following parameters of *DM DG SOI MOSFET* i.e threshold voltage, device capacitance, drain current characteristics, transconductance, drain resistance, cut-off frequency, transit time and noise (thermal and flicker noise).

The dependence of all these parameters on the drain to source voltage, gate to source voltage, channel length, impurity distribution in the silicon layer and the work function difference of the two metals has been studied using the proposed analytical model and also using device simulator program *ATLAS*. It has been found that

1. There is a very close agreement between the results obtained using the analytical model and the same obtained using device simulator. These points to the correctness of the proposed analytical model.
2. That in general the *DM DG MOSFET* offers significantly improve device characteristics. Furthermore in *DM DG* structure the Pearson IV doping distribution in the silicon layer leads to improved device performance.

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Chapter-IV

THE ARTIFICIAL NEURAL NETWORK FOR THE PREDICTION OF THE DEVICE PARAMETERS

4.1 Introduction

Dual-Gate *(DG)* silicon-on-insulator *(SOI) MOSFETs* perhaps the most promising structure for scaling *CMOS* devices down to nanometer sizes. The use of symmetric *DG MOSFETs* having dual-material with ultra-thin bodies and ultra-thin gate oxides allows suppressing the short channel effects, as seen in the previous chapters

There are several approaches for the modeling of semiconductor device characteristics based on the physics of the device as well as numerical techniques. These methods are limited in their applications because of extensive computational requirements or due to lack of accuracy and continuity in the predicted characteristics. So accurate device modeling is important in order to predict the true characteristics of the device. Neural network modeling techniques fill these requirements. Artificial neural networks have the capability to learn from data, to generalize patterns from data and to model non-linear characteristics. These characteristics make neural network techniques an excellent tool in device modeling. Research has been done in device modeling using artificial neural network techniques [121]-[124].

In this work, a back-propagation neural network having five inputs (i.e. silicon layer thickness, oxide layer thickness, channel length, drain-source voltage and gate-source voltage), single hidden layer of eight neurons and five outputs (i.e. surface potential, electric field distribution, drain-current, transconductance and cut-off frequency) are used. A simple, fast and systematic neural network model of *n*-channel *DM DG FD SOI MOSFET* (Figure: 4.1) was developed using Levenberg-Marquardt algorithm. Here, results through device simulator *(ATLAS)* for *DM DG FD SOI* structure are taken as a data through which a neural network is trained and then compared the trained network

with *2-D* analytical model of *DM DG FD SOI MOSFET*. Results are very close which validate our model.

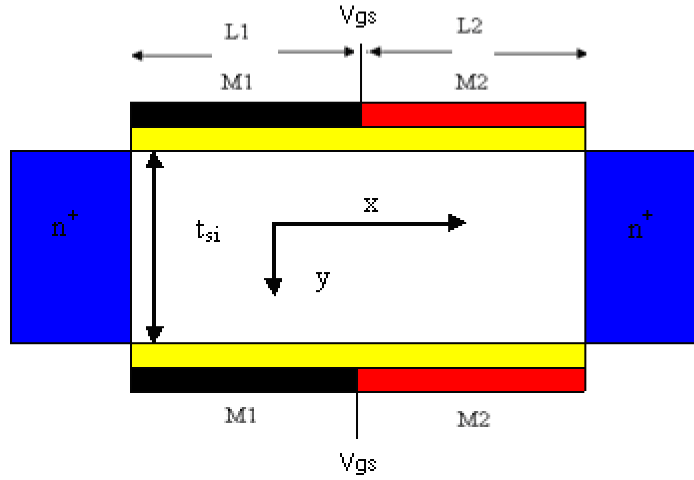

Fig 4.1 Schematic view of n-channel Dual-Material Double-Gate Fully-Depleted SOI MOSFET.

4.2 Model Formulation

A device simulator *ATLAS* is used for the measurement of parameters *i.e.* surface potential (ϕ_s), electric field distribution (E_x), drain-current (I_{ds}), transconductance (g_m) and cut-off frequency (f_c) for dual-material double-gate fully-depleted *SOI MOSFET*. Their comparisons with respective analytical expression have already been shown in the previous chapters. In this model five parameters have been considered although we can increase or decrease the number of parameters used to design *ANN* of the proposed device.

4.2.1 Neural Network Model

A neural network is a machine consisting of interconnected neurons that can be trained by exposure to a certain input pattern along with the desired output to predict the responses to new inputs. Between input and output layers there is a central part of the neural network called a hidden layer. The number of neurons (eight in our case as shown in the figure: 4.2) and hidden layers depends on the complexity of the input response and the desired output.

Consider the weighting matrix between the hidden and input layers as W and the weighting matrix between the output and hidden layer as V, the following can be given:

$$W = [\, w_{nq} \,]_{N.Q} \tag{4.1}$$

where n ϵ (number of input neuron = N = 5) and w_{nq} represents a weighting value between the nth input neuron and the qth hidden neurons and

$$V = [\, v_{qp} \,]_{Q.P} \tag{4.2}$$

where q ϵ (number of hidden neurons = Q = 8), p ϵ (number of output neuron = P = 5) and v_{qp} represent a weighting value between the qth hidden neuron and the pth output neuron. Biases are not shown in the figure just to avoid complexity.

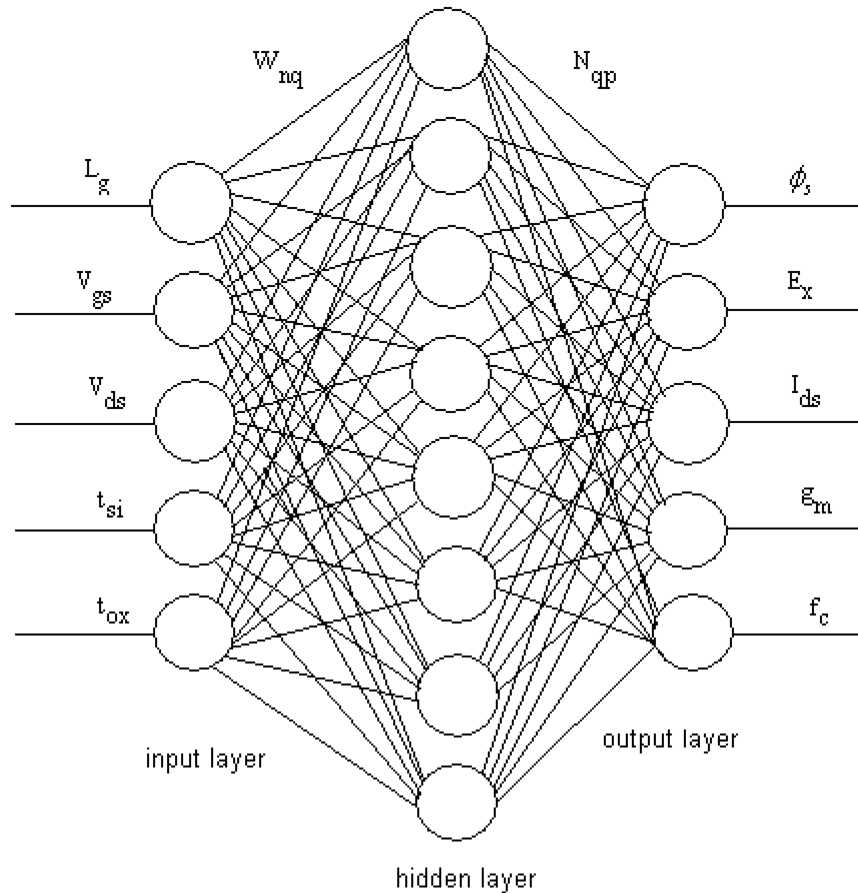

Fig 4.2 Neural network configuration.

4.2.2 Training of the Neural Network

Once the network weights and biases have been initialized, the network is ready for training. The training process requires a set of examples of proper network behavior - network inputs and target outputs.

During training the weights and biases of the neural network are iteratively adjusted to minimize the network performance function as shown in the Figure: 4.3. The performance function is mean square error, *MSE* – the average squared error between the network output and the target output and is defined by

$$E = \sum_{k=1}^{S_d} \left[\frac{1}{2} \left(y^k - z^k \right)^2 \right] \tag{4.3}$$

where, S_d is the total number of data samples, z^k and y^k are desired, or measured and calculated responses. Here the well known Levenberg-Marquardt algorithm in Backpropagation Neural Network along with gradient descent optimization technique, is applied in the neural network training process.

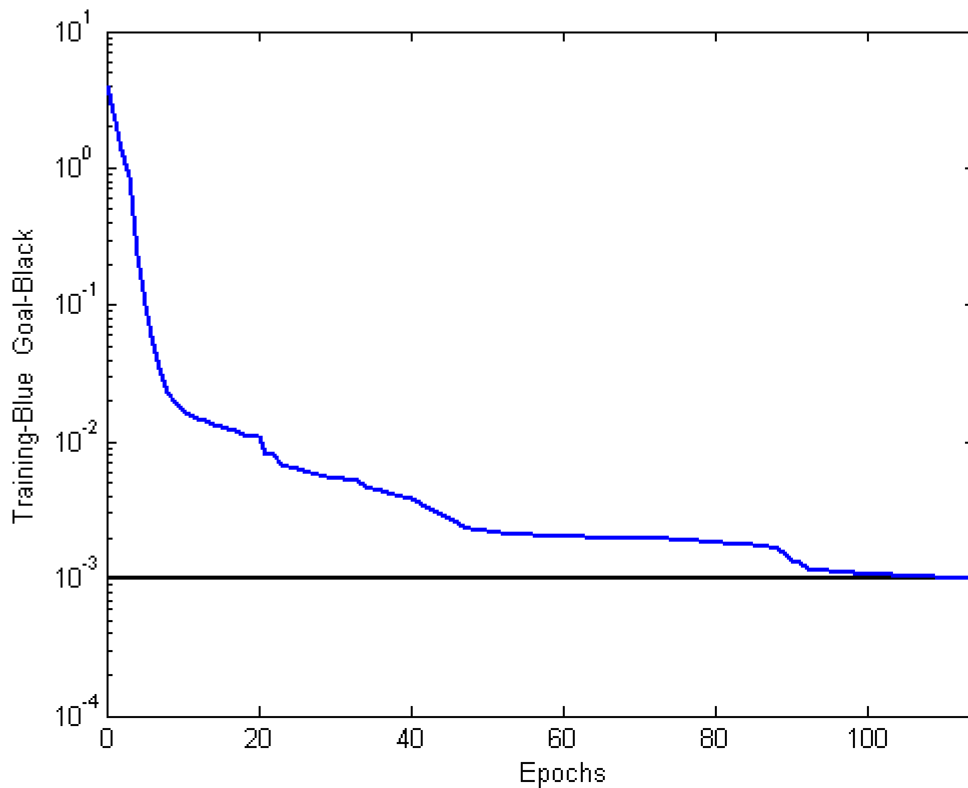

Fig 4.3 Learning curve for Levenberg-Marquardt algorithm in Backpropagation Neural Network for five inputs and five outputs.

The Levenberg-Marquardt algorithm [125] was designed to approach second-order training speed without having to compute the Hessian matrix. When the performance function has the form of a sum of squares (as is typical in training feedforward networks), then the Hessian matrix can be approximated as

$$H = J^T J \tag{4.4}$$

and the gradient can be computed as

$$g = J^T e \tag{4.5}$$

where $\boldsymbol{J}$ is the Jacobian matrix that contains first derivatives of the network errors with respect to the weights and biases, and $\boldsymbol{e}$ is a vector of network errors. The Jacobian matrix can be computed through a standard backpropagation technique that is much less complex than computing the Hessian matrix.

The Levenberg-Marquardt algorithm uses this approximation to the Hessian matrix :

$$x_{k+1} = x_k - [J^T J + \mu . I]^{-1} J^T e \tag{4.6}$$

where x_k is a vector of current weights and biases and x_{k+1} is the one iteration of this algorithm. When the scalar μ is large, this becomes gradient descent with a small step size. Thus μ is decreased after each successful step (reduction in performance function) and is increased only when a tentative step would increase the performance function. In this way, the performance function will always be reduced at each iteration of the algorithm.

The procedure used for neural network modeling of the device proposed is defined as: First initialize weights and threshold values. Feed the neural network with input data (L_g,, V_{ds}, V_g, t_{ox} and t_{si}) along with the respective desired output responses, (ϕ_s , E_x , I_{ds} , g_m and f_c) . Next calculate the *MSE* function by comparing the desired and the calculated output response. Then adjust the weights and threshold values using the updated equations (4.4 - 4.6) so that a certain amount of detected error is removed. Lastly repeat the previous three steps until the error criterion is satisfied.

The accuracy of the neural network modeling increase as the number of training data increase, it has been found that around twenty measurement points for each input and output were sufficient to model the device accurately.

4.3 Results and Discussion

In this work *ANN* model for the *n*-channel *DM DG FD SOI MOSFET* has been proposed. The neural network model developed consists of three layers, input layer is of five

neurons, hidden layer is of eight neurons and output layer is of five neurons. If the training data is sufficient we take less number of neurons in the hidden layer to train the network and vice versa. In this way we optimized the number of neurons in the hidden layer which further optimized the values of weights and biases. The proposed *ANN* model can be used to determine the device surface potential, electric field distribution, drain current, transconductance and cut-off frequency. Also we can use the *ANN* model as an interface between the device modeling and the circuit simulation as it is more flexible, more accurate and much faster than the existing ones. Figures 4.4 – 4.12 show the comparison between the simulator and trained neural network values (trained by set of 100 as well as 20 inputs-outputs data) for surface potential, electric field distribution, drain current, transconductance and cut-off frequency of the *n*-channel *DM DG FD SOI MOSFET*. As there is little difference between the two its mean our neural network model was trained well. This *ANN* model was trained by inputs and outputs having less range but we could also train the same by different sets of inputs and outputs of effective range. After doing so we can test the *ANN* model by selecting the input vector depending on the range of inputs and give it to the trained model, it will give the required outputs based on the optimized weights and biases of the trained neural network. In the broader term, the dynamics of the proposed device is fully captured by the artificial neural network which would help to predict the behavior of the device in terms of five output parameters.

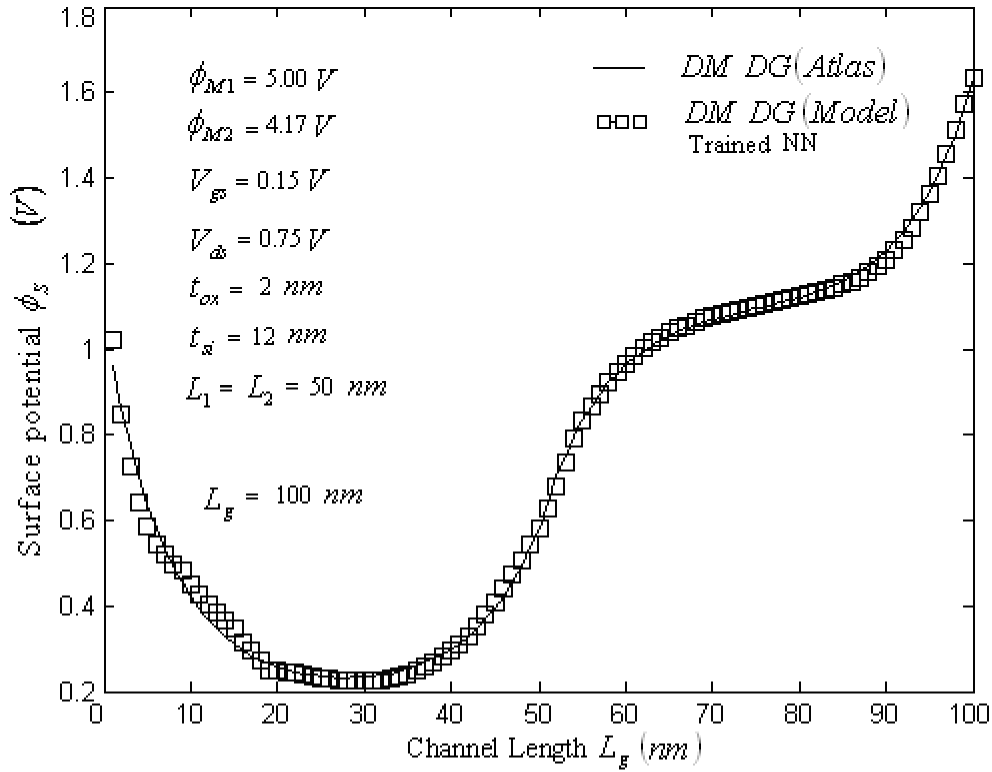

Fig 4.4 Comparison between device simulator and trained neural network model of DM DG FD SOI MOSFET for surface potential (trained by set of 100 inputs-outputs data)

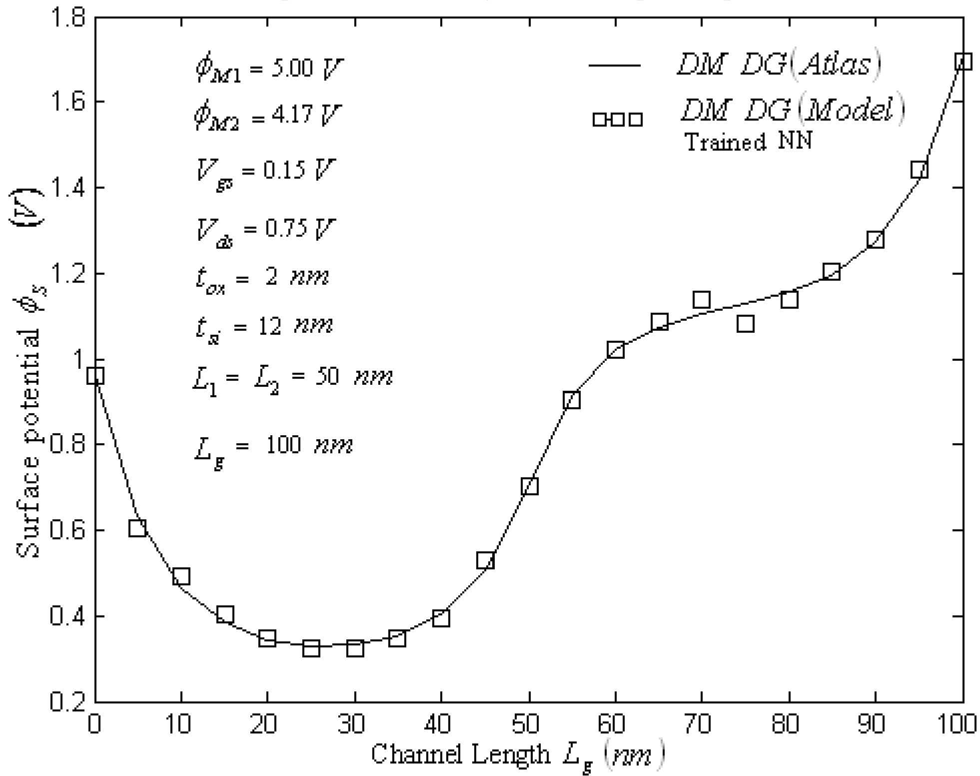

Fig 4.5 Comparison between Simulator and trained neural network model of DM DG FD SOI MOSFET for surface potential (trained by set of 20 inputs-outputs data).

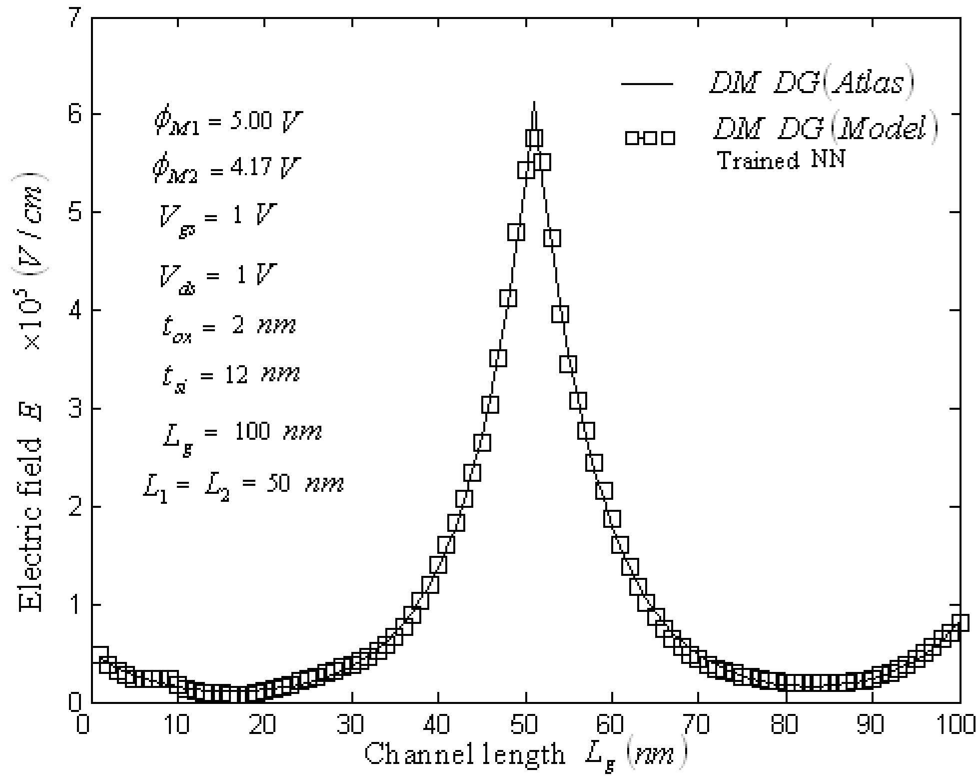

Fig 4.6 Comparison between device simulator and trained neural network model of DM DG FD SOI MOSFET for electric-field distribution (trained by set of 100 inputs-outputs data).

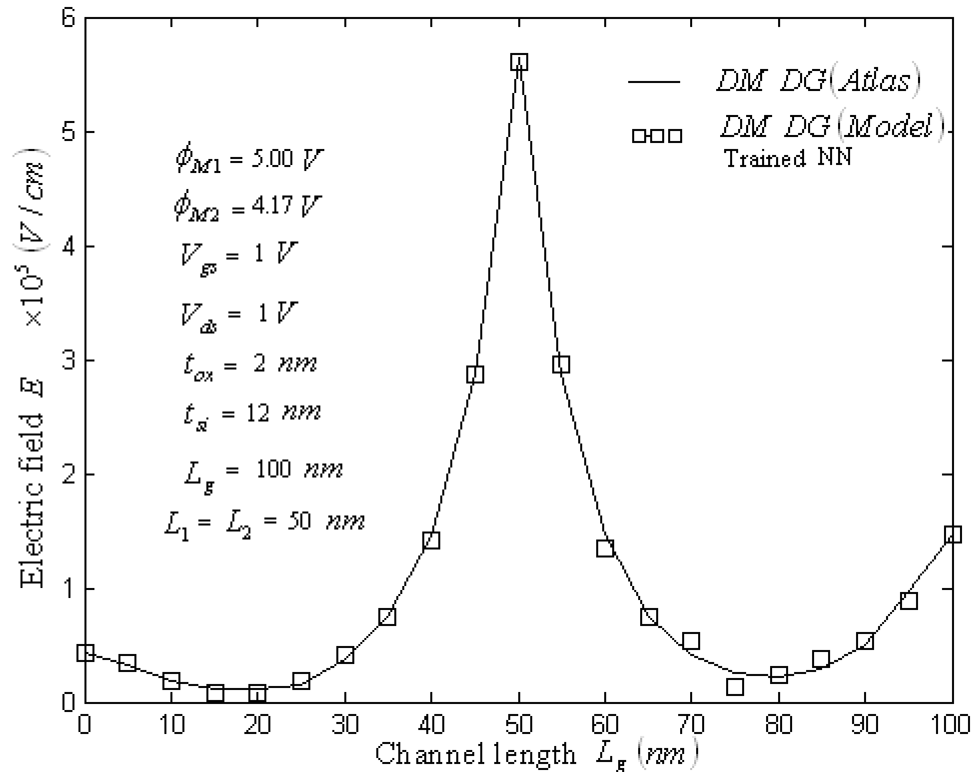

Fig 4.7 Comparison between device simulator and trained neural network model of DM DG FD SOI MOSFET for electric-field distribution (trained by set of 20 inputs-outputs data).

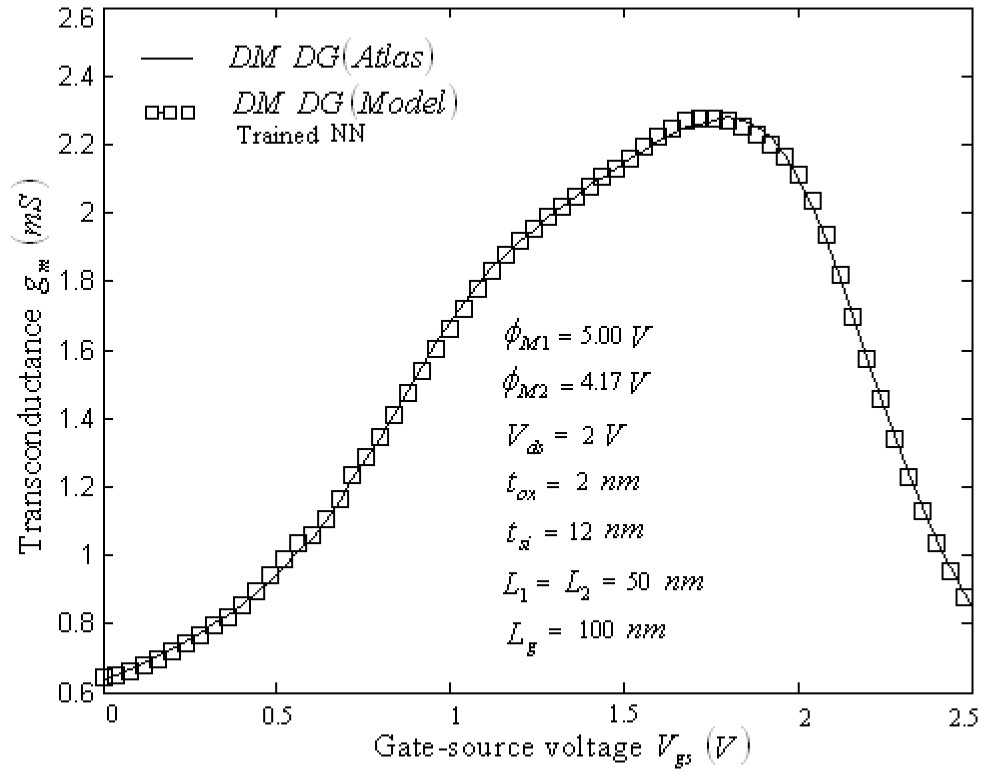

Fig 4.8 Comparison between device simulator and trained neural network model of DM DG FD SOI MOSFET for transconductance (trained by set of 100 inputs-outputs data).

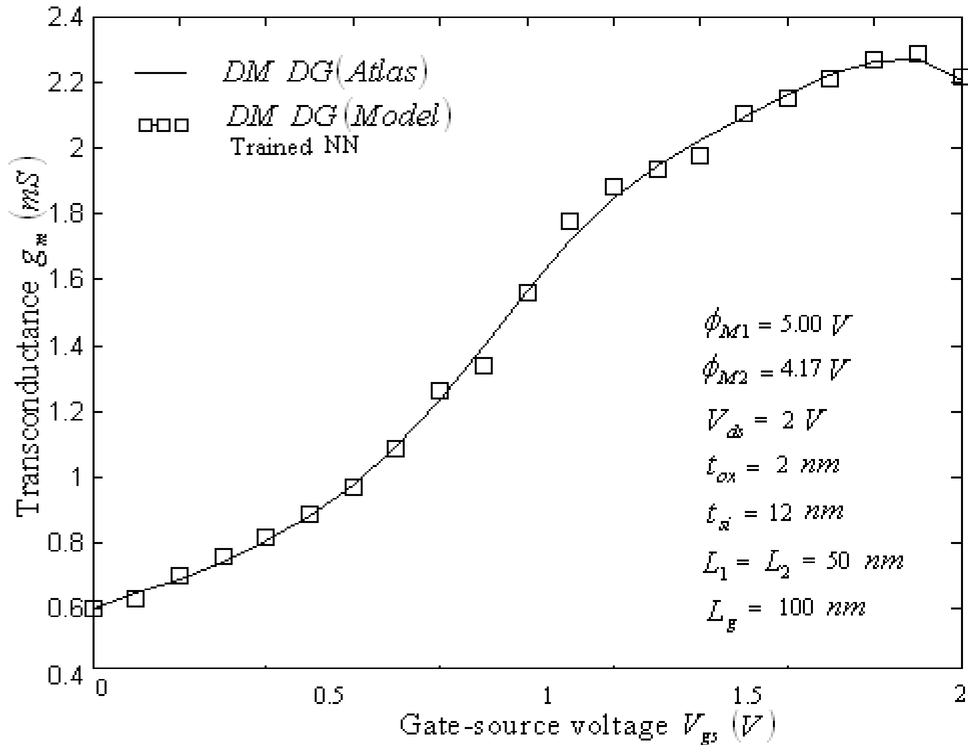

Fig 4.9 Comparison between device simulator and trained neural network model of DM DG FD SOI MOSFET for transconductance (trained by set of 20 inputs-outputs data).

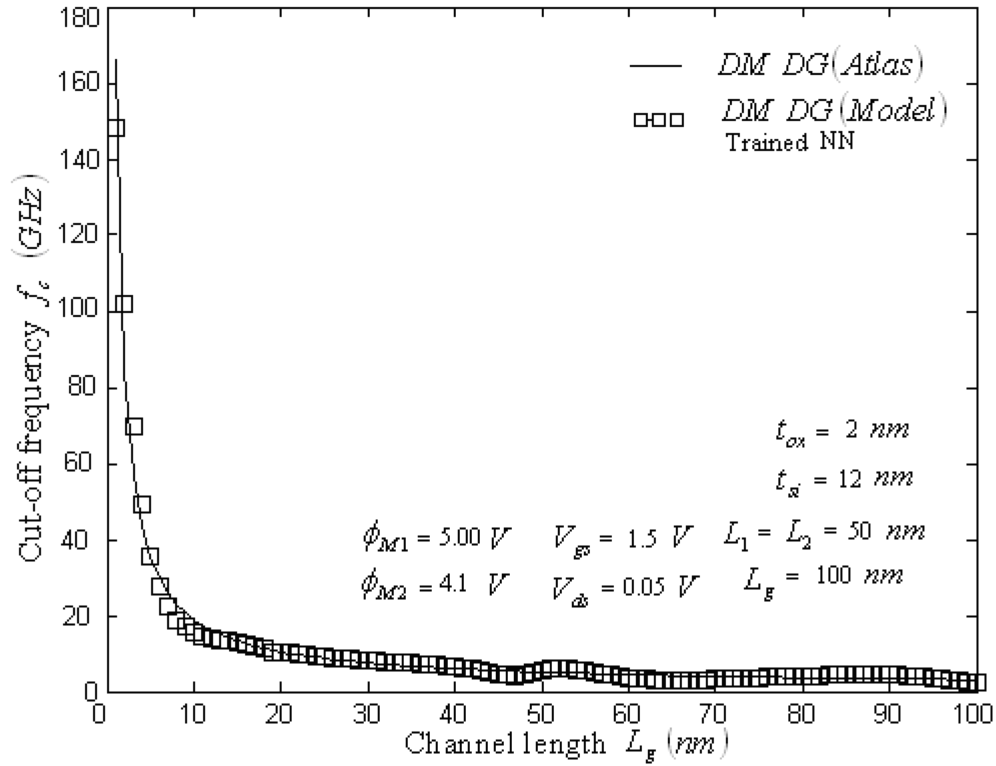

Fig 4.10 Comparison between device simulator and trained neural network model of DM DG FD SOI MOSFET for transconductance (trained by set of 100 inputs-outputs data).

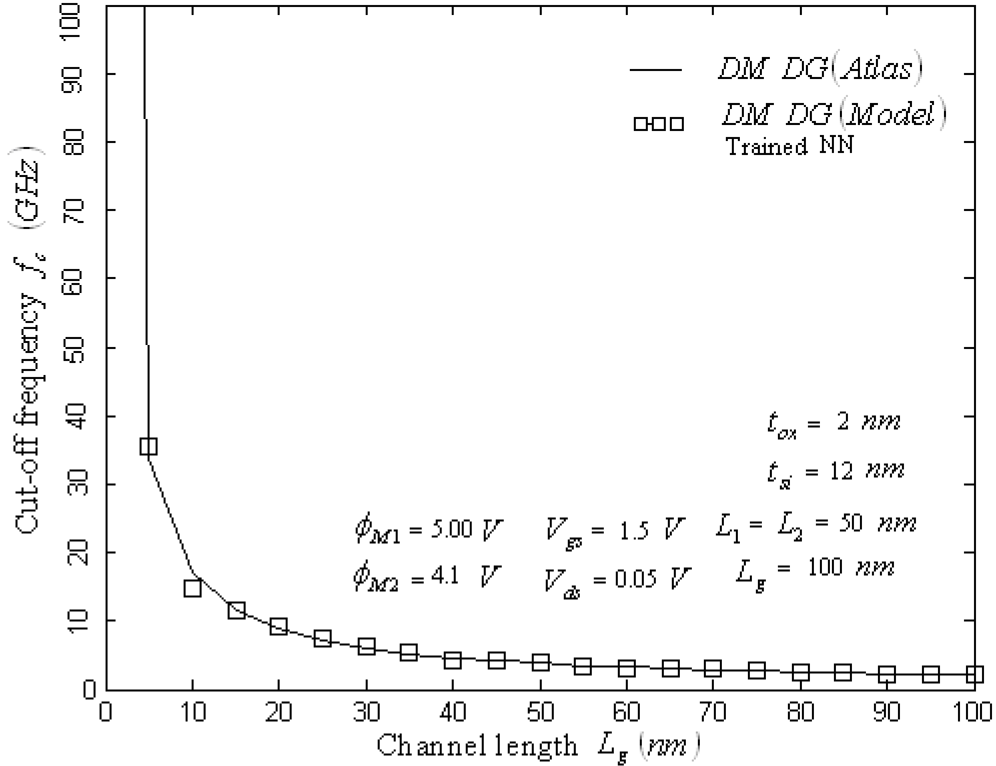

Fig 4.11 Comparison between device simulator and trained neural network model of DM DG FD SOI MOSFET for transconductance (trained by set of 20 inputs-outputs data).

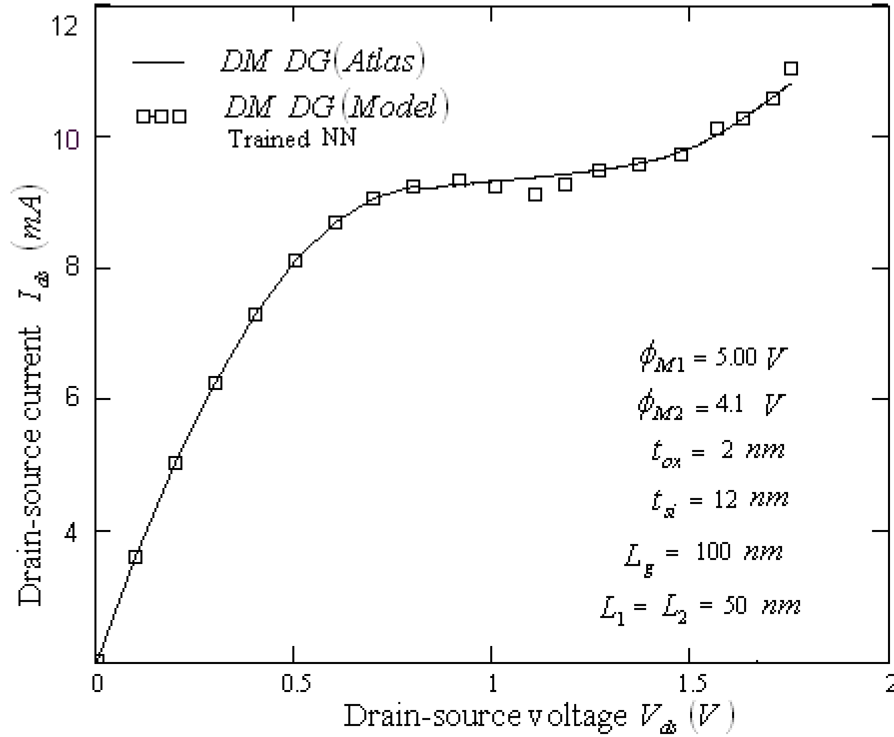

Fig 4.12 Comparison between device simulator and trained neural network model of DM DG FD SOI MOSFET for drain-source current (trained by set of 20 inputs-outputs data).

4.4 Summary

A neural network was trained and used to model *n*-channel *DM DG FD SOI MOSFET* characteristics (surface potential (ϕ_s), electric field distribution (E_x), drain-current (I_{ds}), transconductance (g_m) and cut-off frequency (f_c)) for different combinations of silicon layer thickness (t_{si}), oxide layer thickness (t_{ox}), channel length ($L_g = L_1 + L_2$), drain-source voltage (V_{ds})and gate-source voltage (V_{gs}) within the operational range of the device. After training, the dynamics or behavior of the proposed device is captured by the *ANN*. Now output can be predicted for any combination of the input parameters within the feasible range. The output predicted depends upon the optimized weights and biases. Here optimization was done using Levenberg-Marquardt method. The main advantage of applying a Levenberg-Marquardt algorithm in Backpropagation Neural Network in device modeling was that only a small number of target data was sufficient to quickly and

accurately model the device. The model provides good insight into the device structure optimization and performance prediction.

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Chapter-V

CONCLUSION AND FUTURE SCOPE OF WORK

5.1 CONCLUSION

The bulk *Si MOSFET* has been the main device forming the backbone of the development of ultra high density *ICs*. However, due to continuous miniaturization, a situation has reached, where the performance parameters of the *MOSFETs* are degraded (due to the basic physical limits), to the extent that it is very difficult to fabricate *ICs* with nano-scale bulk *MOSFETs*. A new generation device, which can offer good performance parameters i.e. low power consumption and high speed, even for nano-sacle devices, is required. As discussed in Chapter-I, *DG SOI MOSFET* followed by dual-material (which offers improved electron transport efficiency), is one such alternative.

For *IC* design, it is essential to have an accurate device model describing the electrical behavior of the device. This require the exact solution of the basic semiconductor equation i.e. Poisson's equation, continuity equation, current transport equation and other related equations. The solution of these equations invariably involved numerical analysis. The situation becomes even more complex for nano-sacle devices where the equations are to be considered in *2-D* or *3-D*. In such situations, an analytical model which can give approximately same results as may be obtained by exact numerical analysis would be very useful, provided the results obtained from the analytical model are same as those obtained by numerical solution within acceptable tolerance. Also, for improved device performance the body region is doped by ion implantation process. For this, the device behavior needs to be analyzed assuming a doping distribution as close to practically obtained doping distribution (i.e. Pearson IV) as possible.

In this work, attempt has been made to develop *2-D* analytical models with Pearson IV type doping distribution for the following parameters of *DM DG FD SOI MOSFET* : potential distribution, electric field distribution, electron velocity distribution, subthreshold swing, threshold voltage, device capacitance, drain-current,

transconductance, drain resistance, cut-off frequency, transit time and noise – thermal & flicker noise. The dependence of all these parameters on the drain to source voltage, gate to source voltage, channel length, impurity distribution in the silicon layer and the work function difference of the two metals has been studied using the proposed analytical model and also using device simulator program *ATLAS*.

It has been observed that

1. In case of *DM DG SOI MOSFET*, the source is effectively screened from the variation in the drain voltage due to step function profile of the potential at the interface of metals M1 and M2. The electric field is reduced near the drain leading to reduction in hot carrier effect. The reduction in electric field near the drain is also found to be dependent upon the difference between the work function of the two metals. As the difference between the work functions of the two metal increases the electric field near the drain decreases.
2. The effect of *DIBL* is considerably reduced in case of *DM DG SOI MOSFET*.
3. The nature of impurity distribution also affects the potential and electric field distribution and therefore the device characteristics.
4. The peak electron velocity is higher in case of *DM DG SOI* structure in comparison to the same for *SM DG SOI* structure.
5. Better control on threshold voltage in case of *DM DG SOI* structure in comparison to the same for *SM DG SOI* structure for small channel lengths.
6. The depletion capacitance is much smaller in case of *DM DG* structure (in comparison to same for *SM DG*) particularly for a small value of gate to source voltage. This is expected because in *SM DG* structure the metal chosen had larger work function.
7. The drain current increases with increase in the gate metal work function difference.
8. Transconductance is significantly larger in case of *DM DG SOI* structure indicating that the gate has better control over the conductance in case *DM DG SOI* structure. It is also observed that larger the work functions difference larger is transconductance.

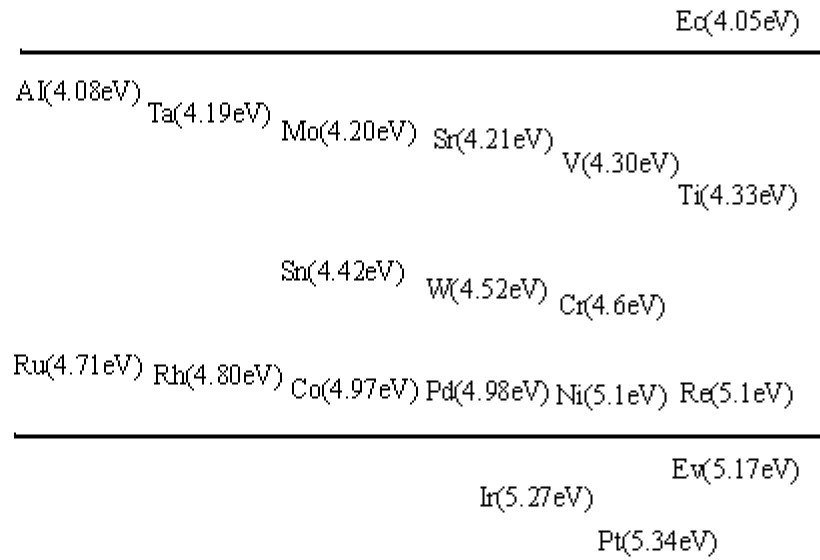
9. The drain-resistance in case of *DM DG SOI* structure is lower than that in case of *SM DG SOI* structure. This is consistent with higher current drive capability of the *DM DG SOI* structure.
10. The cut-off frequency decreases with increasing channel length. The *DM DG* structure offers higher cut-off frequency because of higher transconductance of *DM DG* structure.
11. The proposed structure offers improved noise (thermal & flicker noise) behavior over *SM DG* structure.
12. The calculated results using the analytical expressions are in excellent agreement with the simulation results (obtained using device simulator *ATLAS*).
13. An artificial neural network model of the proposed device has been developed using Levenberg-Marquardt algorithm. It can predict the device characteristics for a given *DM DG FD SOI MOSFET* structure without going into complex computations.

5.2 Future Scope of the Work

Different gate structures along with *SOI* wafer technology are now viewed as the most important emerging engineering technology for use in leading edge *CMOS IC* production during the next 3-5 years. One plausible scenario during this period is the rapid adoption of *SOI* wafers in place of single crystal silicon wafers now employed as starting substrates for high-end logic device (e.g., microprocessors) and *SOC* (**S**ystem **O**n **C**hip) applications at the *0.13* and *0.10 micron* technology nodes. *SOI* technology appear to offer an excellent platform for integrating *RF* and digital circuits on the same chip due to its superior *RF*/ high speed performance.

Appendix: A

The workfunction of the common metals in the silicon bandgap



Appendix: B

Simplification of 2D Poisson's equation for $\phi_1(x,y)$ and $\phi_2(x,y)$ in one dimensional equation in $\phi_{c1}(x)$ and $\phi_{c2}(x)$

Substituting $\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{oxf}} = A_1$ and $\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{oxf}} = B_1$ in equations (2.40) & (2.41), we get

$$\phi_1(x,y) = \left(1 + B_1 \cdot y - \frac{B_1}{t_{si}} \cdot y^2\right)\left(\frac{1}{1+A_1}\left(\phi_{c1}(x) + A_1.V'_{gs11}\right)\right) - B_1.V'_{gs1} \cdot y + \frac{B_1}{t_{si}} \cdot V'_{gs1}.y^2 \tag{b1.0}$$

$$\phi_2(x,y) = \left(1 + B_1 \cdot y - \frac{B_1}{t_{si}} \cdot y^2\right)\left(\frac{1}{1+A_1}\left(\phi_{c2}(x) + A_1.V'_{gs22}\right)\right) - B_1.V'_{gs2} \cdot y + \frac{B_1}{t_{si}} \cdot V'_{gs2}.y^2 \tag{b1.1}$$

Differentiating equations (b1.0) & (b1.1) with respect to x, we get

$$\frac{\partial \phi_1(x,y)}{\partial x} = \left(1 + B_1 \cdot y - \frac{B_1}{t_{si}} \cdot y^2\right)\left(\frac{1}{1+A_1}\frac{d\phi_{c1}(x)}{dx}\right) \tag{b1.2}$$

$$\frac{\partial \phi_2(x,y)}{\partial x} = \left(1 + B_1 \cdot y - \frac{B_1}{t_{si}} \cdot y^2\right)\left(\frac{1}{1+A_1}\frac{d\phi_{c2}(x)}{dx}\right) \tag{b1.3}$$

Differentiating again equations (b1.2) & (b1.3) with respect to x, we get

$$\frac{\partial^2 \phi_1(x,y)}{\partial x^2} = \left(1 + B_1 \cdot y - \frac{B_1}{t_{si}} \cdot y^2\right)\left(\frac{1}{1+A_1}\frac{d^2\phi_{c1}(x)}{dx^2}\right) \tag{b1.4}$$

$$\frac{\partial^2 \phi_2(x,y)}{\partial x^2} = \left(1 + B_1 \cdot y - \frac{B_1}{t_{si}} \cdot y^2\right)\left(\frac{1}{1+A_1}\frac{d^2\phi_{c2}(x)}{dx^2}\right) \tag{b1.5}$$

Now differentiating equations (b1.0) & (b1.1) with respect to y, we get

$$\frac{\partial \phi_1(x,y)}{\partial y} = \left(B_1 - 2.\frac{B_1}{t_{si}} \cdot y \right)\left(\frac{1}{1+A_1}\left(\phi_{c1}(x) + A_1.V'_{gs11}\right)\right) - B_1.V'_{gs1} + 2.\frac{B_1}{t_{si}}.V'_{gs1} \cdot y \qquad \text{(b1.6)}$$

$$\frac{\partial \phi_2(x,y)}{\partial y} = \left(B_1 - 2.\frac{B_1}{t_{si}} \cdot y \right)\left(\frac{1}{1+A_1}\left(\phi_{c2}(x) + A_1.V'_{gs22}\right)\right) - B_1.V'_{gs2} + 2.\frac{B_1}{t_{si}}.V'_{gs2} \cdot y \qquad \text{(b1.7)}$$

Differentiating again equations (b1.6) & (b1.7) with respect to y, we get

$$\frac{\partial^2 \phi_1(x,y)}{\partial y^2} = \left(-2.\frac{B_1}{t_{si}} \right)\left(\frac{1}{1+A_1}\left(\phi_{c1}(x) + A_1.V'_{gs11}\right)\right) + 2.\frac{B_1}{t_{si}}.V'_{gs1} \qquad \text{(b1.8)}$$

$$\frac{\partial^2 \phi_2(x,y)}{\partial y^2} = \left(-2.\frac{B_1}{t_{si}} \right)\left(\frac{1}{1+A_1}\left(\phi_{c2}(x) + A_1.V'_{gs22}\right)\right) + 2.\frac{B_1}{t_{si}}.V'_{gs2} \qquad \text{(b1.9)}$$

Substituting equations (b1.4), (b1.5), (b1.8) and (b1.9) into equation (2.12), we get

$$\frac{\partial^2 \phi_1(x,y)}{\partial x^2} + \frac{\partial^2 \phi_1(x,y)}{\partial y^2} = \frac{q \cdot N_a(y)}{\varepsilon_{si}} \qquad \text{for} \quad 0 \le x \le L_1 \quad \text{and} \quad 0 \le y \le t_{si}$$

or

$$\left(1 + B_1 \cdot y - \frac{B_1}{t_{si}} \cdot y^2 \right)\left(\frac{1}{1+A_1} \frac{d^2\phi_{c1}(x)}{dx^2} \right) - 2.\frac{B_1}{t_{si}}\left(\frac{1}{1+A_1}\left(\phi_{c1}(x) + A_1.V'_{gs11}\right)\right) + 2.\frac{B_1}{t_{si}}.V'_{gs1} = \frac{q.N_a(y)}{\varepsilon_{si}}$$

(b1.10)

and

$$\frac{\partial^2\phi_2(x,y)}{\partial x^2}+\frac{\partial^2\phi_2(x,y)}{\partial y^2}=\frac{q\cdot N_a(y)}{\varepsilon_{si}} \qquad \text{for} \quad L_1 \le x \le L_1+L_2 \quad \text{and} \quad 0 \le y \le t_{si}$$

or

$$\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\left(\frac{1}{1+A_1}\frac{d^2\phi_{c2}(x)}{dx^2}\right)-2.\frac{B_1}{t_{si}}\left(\frac{1}{1+A_1}\left(\phi_{c2}(x)+A_1.V_{gs22}^{'}\right)\right)+2.\frac{B_1}{t_{si}}.V_{gs2}^{'} =\frac{q.N_a(y)}{\varepsilon_{si}}$$

(b1.11)

On further solving equations (b1.10) and (b1.11), we get

$$\frac{d^2\phi_{c1}(x)}{dx^2}-\frac{2.\frac{B_1}{t_{si}}\frac{1}{1+A_1}}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}\phi_{c1}(x) = \frac{\frac{q.N_a(y)}{\varepsilon_{si}}}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}+\frac{\left(2.\frac{B_1}{t_{si}}\frac{1}{1+A_1}A_1.V_{gs11}^{'}-2.\frac{B_1}{t_{si}}.V_{gs1}^{'}\right)}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}$$

(b1.12)

and

$$\frac{d^2\phi_{c2}(x)}{dx^2}-\frac{2.\frac{B_1}{t_{si}}\frac{1}{1+A_1}}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}\phi_{c1}(x) = \frac{\frac{q.N_a(y)}{\varepsilon_{si}}}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}+\frac{\left(2.\frac{B_1}{t_{si}}\frac{1}{1+A_1}A_1.V_{gs22}^{'}-2.\frac{B_1}{t_{si}}.V_{gs2}^{'}\right)}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}$$

(b1.13)

On further simplification of above equations, we get

$$\frac{d^2\phi_{c1}(x)}{dx^2}-\frac{2.\frac{B_1}{t_{si}}\frac{1}{1+A_1}}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}\phi_{c1}(x) = \frac{\frac{q.N_a(y)}{\varepsilon_{si}}+\left(2.\frac{B_1}{t_{si}}\frac{1}{1+A_1}A_1.V'_{gs11}-2.\frac{B_1}{t_{si}}.V'_{gs1}\right)}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}$$

(b1.14)

$$\frac{d^2\phi_{c2}(x)}{dx^2}-\frac{2.\frac{B_1}{t_{si}}\frac{1}{1+A_1}}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}\phi_{c2}(x)$$

$$= \frac{\frac{q.N_a(y)}{\varepsilon_{si}}+\left(2.\frac{B_1}{t_{si}}\frac{1}{1+A_1}A_1.V'_{gs22}-2.\frac{B_1}{t_{si}}.V'_{gs2}\right)}{\left(\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\frac{1}{1+A_1}\right)}$$

(b1.15)

We can write equations (b1.14) & (b1.11) as

$$\left(\frac{d^2\phi_{c1}(x)}{dx^2}\right)-\frac{1}{\frac{\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)}{2.\frac{B_1}{t_{si}}}}\left(\phi_{c1}(x)+A_1.V'_{gs11}-(1+A_1)V'_{gs1}\right) = \frac{\frac{q.N_a(y)}{\varepsilon_{si}}}{\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\left(\frac{1}{1+A_1}\right)}$$

(b1.16)

$$\left(\frac{d^2\phi_{c2}(x)}{dx^2}\right)-\frac{1}{\frac{\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)}{2.\frac{B_1}{t_{si}}}}\left(\phi_{c2}(x)+A_1.V'_{gs22}-(1+A_1)V'_{gs2}\right) = \frac{\frac{q.N_a(y)}{\varepsilon_{si}}}{\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)\left(\frac{1}{1+A_1}\right)}$$

(b1.17)

Simplify further

$$\left(\frac{d^2\phi_{c1}(x)}{dx^2}\right)-\frac{1}{\lambda_1^2}\left(\phi_{c1}(x)+A_1.V'_{gs11}-(1+A_1)V'_{gs1}\right) = \frac{q.N_a(y)}{\varepsilon_{si}}.\frac{1}{\lambda^2{}_{11}} \qquad \text{(b1.18)}$$

and

$$\left(\frac{d^2\phi_{c2}(x)}{dx^2}\right)-\frac{1}{\lambda_1^2}\left(\phi_{c2}(x)+A_1.V'_{gs22}-(1+A_1)V'_{gs2}\right) = \frac{q.N_a(y)}{\varepsilon_{si}}.\frac{1}{\lambda^2{}_{11}} \qquad \text{(b1.19)}$$

where

$$\lambda_1^2 = \frac{\left(1+B_1\cdot y-\frac{B_1}{t_{si}}\cdot y^2\right)}{2.\frac{B_1}{t_{si}}} \quad \text{and} \quad \lambda^2{}_{11} = \left(1+\frac{\varepsilon_{ox}}{\varepsilon_{si}.t_{ox}}\cdot y-\frac{1}{t_{si}}.\frac{\varepsilon_{ox}}{\varepsilon_{si}.t_{ox}}\cdot y^2\right)\left(\frac{1}{1+\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{ox}}}\right)$$

At $y=\frac{t_{si}}{2}$,

$$\lambda_1^2 = \frac{\left(1+\frac{\varepsilon_{ox}}{\varepsilon_{si}.t_{ox}}\cdot\frac{t_{si}}{2}-\frac{1}{t_{si}}.\frac{\varepsilon_{ox}}{\varepsilon_{si}.t_{ox}}\cdot\left(\frac{t_{si}}{2}\right)^2\right)}{2.\frac{1}{t_{si}}.\frac{\varepsilon_{ox}}{\varepsilon_{si}.t_{ox}}}$$

$$\lambda^2{}_1 = \frac{\varepsilon_{si}.t_{ox}.t_{si}}{2.\varepsilon_{ox}}+\frac{t^2{}_{si}}{8}\;; \qquad \text{or} \qquad \lambda_1 = \sqrt{\frac{\varepsilon_{si}.t_{ox}.t_{si}}{2.\varepsilon_{ox}}+\frac{t^2{}_{si}}{8}} \qquad \text{(b1.20)}$$

and $$\lambda^2{}_{11} = \left(1+\frac{\varepsilon_{ox}}{\varepsilon_{si}.t_{ox}}\cdot\left(\frac{t_{si}}{2}\right)-\frac{1}{t_{si}}.\frac{\varepsilon_{ox}}{\varepsilon_{si}.t_{ox}}\cdot\left(\frac{t_{si}}{2}\right)^2\right)\left(\frac{1}{1+\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{ox}}}\right)$$

$$\lambda^2{}_{11} = 1 \; ; \tag{b1.21}$$

Appendix: C

Calculations of equations for $A_{011}, A_{022}, B_{011}$ and B_{022}.

From equation (2.23), we get

$$\phi_1(L_1,0) = \left(1+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{t_{ox}}\cdot 0-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{t_{ox}.t_{si}}\cdot(0)^2\right)\left(\frac{1}{1+\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{ox}}}\left(\phi_{c1}(L_1)+\frac{\varepsilon_{ox}.t_{si}.V'_{gs11}}{4.\varepsilon_{si}.t_{ox}}\right)\right) - \frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{V'_{gs1}}{t_{ox}}\cdot 0+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{V'_{gs1}}{t_{ox}.t_{si}}\cdot(0)^2 \quad \text{(c1.0)}$$

$$\phi_2(L_1,0) = \left(1+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{t_{ox}}\cdot 0-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{t_{ox}.t_{si}}\cdot(0)^2\right)\left(\frac{1}{1+\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{ox}}}\left(\phi_{c2}(L_1)+\frac{\varepsilon_{ox}.t_{si}.V'_{gs22}}{4.\varepsilon_{si}.t_{ox}}\right)\right) - \frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{V'_{gs2}}{t_{ox}}\cdot 0+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{V'_{gs2}}{t_{ox}.t_{si}}\cdot(0)^2 \quad \text{(c1.1)}$$

By equating above two equations (c1.0) and (c1.1), we get

$$\left(\phi_{c1}(L_1)+A_1.V'_{gs11}\right)=\left(\phi_{c2}(L_1)+A_1.V'_{gs22}\right) \quad \text{(c1.2)}$$

Substituting values for $\phi_{c1}(L_1)$ & $\phi_{c2}(L_1)$ from equations (2.56) & (2.57) in equation (c1.2), we get

$$\left((1+A_1)V'_{gs1}\right)-\frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\,2}+A_{011}.\exp\left(\frac{L_1}{\lambda_1}\right)+B_{011}.\exp\left(\frac{-L_1}{\lambda_1}\right) = \left((1+A_1)V'_{gs2}\right)-\frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\,2}+A_{022}+B_{022} \quad \text{(c1.3)}$$

or $$A_{011}.\exp\left(\frac{L_1}{\lambda_1}\right)+B_{011}.\exp\left(\frac{-L_1}{\lambda_1}\right)-A_{022}-B_{022}=-(\gamma_1-\gamma_2) \quad \text{(c1.4)}$$

where $$\gamma_1 = \left((1+A_1)V'_{gs1}\right)-\frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\,2} \text{ and} \quad \text{(c1.5)}$$

$$\gamma_2 = \left((1+A_1)V'_{gs2}\right)-\frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\,2} \quad \text{(c1.6)}$$

Using equation (2.24), we get

$$\left.\frac{d\phi_{c1}(x)}{dx}\right|_{x=L_1} = \left.\frac{d\phi_{c2}(x)}{dx}\right|_{x=L_1}$$

On differentiating equations (2.56) & (2.57) w.r.t x and equating them futher at $x = L_1$, we get

$$A_{011}.\exp\left(\frac{L_1}{\lambda_1}\right)-B_{011}.\exp\left(\frac{-L_1}{\lambda_1}\right)-A_{022}+B_{022}=0 \quad \text{(c1.7)}$$

Using equation (2.25), we get

$$\phi_{s1}(0)=\frac{1}{1+A_1}\left(\left((1+A_1)V'_{gs1}\right)-\frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda_1^{\,2}+A_{011}.\exp\left(\frac{0}{\lambda_1}\right)+B_{011}.\exp\left(\frac{-0}{\lambda_1}\right)\right)$$

$$= \frac{1}{1+A_1}(\gamma_1+A_{011}+B_{011})$$

or

$$\frac{1}{1+A_1}(\gamma_1+A_{011}+B_{011}) = V_{bi}; \qquad \text{or} \qquad A_{011}+B_{011} = V_{bi}(1+A_1)-\gamma_1 \quad \text{(c1.8)}$$

Using equation (2.26) in equation (2.59), we get

$$\phi_{s2}(L_1+L_2)=\frac{1}{1+A_1}\left(\gamma_2+A_{022}.\exp\left(\frac{(L_2)}{\lambda_1}\right)+B_{022}.\exp\left(\frac{-(L_2)}{\lambda_1}\right)\right)=V_{bi}+V_{ds} \qquad \text{or}$$

$$A_{022}.\exp\left(\frac{(L_2)}{\lambda_1}\right)+B_{022}.\exp\left(\frac{-(L_2)}{\lambda_1}\right)=(V_{bi}+V_{ds}).(1+A_1)-\gamma_2 \quad \text{(c1.9)}$$

Solving equations (c1.4), (c1.7), (c1.8) & (c1.9) for A_{011}, A_{022}, B_{011} and B_{022}, we get

$$A_{011} = -\frac{1}{2}\frac{2.S.\exp\left(-\frac{L_1}{\lambda_1}\right) - 2.T_o.\exp\left(\frac{L_2}{\lambda_1}\right) - R - \exp\left(\frac{2L_2}{\lambda_1}\right).R}{\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - \exp\left(-\frac{L_1}{\lambda_1}\right)} \tag{c1.10}$$

and

$$B_{011} = \frac{2.S.\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - 2.T_o.\exp\left(\frac{L_2}{\lambda_1}\right) - R - \exp\left(\frac{2L_2}{\lambda_1}\right).R}{2.\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - 2.\exp\left(-\frac{L_1}{\lambda_1}\right)} \tag{c1.11}$$

$$A_{022} = -\frac{1}{2}\frac{\begin{pmatrix} -2.S + 2.\exp\left(\frac{L_1+L_2}{\lambda_1}\right).T_o + \exp\left(\frac{L_1}{\lambda_1}\right).R - R.\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) + 2.\exp\left(\frac{2L_2}{\lambda_1}\right).S + \\ \exp\left(-\frac{L_1}{\lambda_1}\right).R - \exp\left(-\frac{(L_1-2L_2)}{\lambda_1}\right).R - 2.T_o\exp\left(\frac{L_1+3L_2}{\lambda_1}\right) \end{pmatrix}}{\left(\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - \exp\left(-\frac{L_1}{\lambda_1}\right)\right)\left(-1+\exp\left(\frac{2L_2}{\lambda_1}\right)\right)} \tag{c1.12}$$

$$B_{022} = -\frac{1}{2}\frac{\begin{pmatrix} -2.T_0.\exp\left(-\frac{L_1}{\lambda_1}\right) + 2.T_o.\exp\left(-\frac{(L_1-2L_2)}{\lambda_1}\right) + 2.\exp\left(\frac{(L_2)}{\lambda_1}\right).S - \\ \exp\left(\frac{L_1+L_2}{\lambda_1}\right).R + \exp\left(\frac{L_1+3L_2}{\lambda_1}\right).R - 2.\exp\left(\frac{3L_2}{\lambda_1}\right).S - \\ \exp\left(\frac{L_2-L_1}{\lambda_1}\right).R + \exp\left(\frac{-L_1+3L_2}{\lambda_1}\right).R \end{pmatrix}.\exp\left(\frac{L_2}{\lambda_1}\right)}{\left(\exp\left(\frac{L_1+2L_2}{\lambda_1}\right) - \exp\left(-\frac{L_1}{\lambda_1}\right)\right)\left(-1+\exp\left(\frac{2L_2}{\lambda_1}\right)\right)} \tag{c1.13}$$

where $$R = -(\gamma_1 - \gamma_2); \tag{c1.14}$$

$$S = V_{bi}(1 + A_1) - \gamma_1; \tag{c1.15}$$

$$T_o = (V_{bi} + V_{ds}).(1 + A_1) - \gamma_2 \tag{c1.16}$$

Appendix: D

Details of threshold voltage

Substituting $\phi_{s1}\left(x_{\min},\frac{t_{si}}{2}\right)=2.\phi_F$ and $V_{gs}=V_{th}$ into equation (2.71), the threshold voltage (equation (3.1)) obtained is given as

$$V_{th}=\frac{-G7+\sqrt{G7^2-4.G6.G8}}{2.G6}$$

where $G8 = F5+F8-G2-G5$; $G7=F4-F7-G1-G4$;

$G6=F3+F6-F9-G3$; $G3=4E3^2.E7.(1+A_1)^2$;

$G5=4.E3^2.F2^2.E7+(2..E3.F2-2.E5.F1+2.F2.E3+R\ .E4\ ).E7.R\ .E4$;

$G4=(-8.F2.E7.E3^2-2.R.E4.E3.E7+2.R.E5.E4.E7-2.R.E3.E4.E7).(1+A_1)$;

$G2=(4.E2.E5.F1\ -4.F2.E3.E5-2.R.E4.E5-4.E2.E3.F2)F1.E7$;

$G1=C2+(2.E7.R.E4.E5+4.E7.E2.E3.F1+4.E7.E2.E3.F2).(1+A_1)$;

$C2=(-8.E2.E5.E7.F1+4.E7.F1.E3.E5+4.E7.F2.E3.E5).(1+A_1)$;

$F9=4.(E7.E2.E5-E7.E3.E5-E7.E2.E3).(1+A_1)^2$;

$F7=C1+4.(-2.E6.E2.E3.F2-E6E2.R.E4+E6.E3.R.E4).(1+A_1)$;

$$F8=4.\begin{pmatrix}E2^2.E6.F1^2+E3^2.E6.F2^2-2.E6.E2.E3.F1.F2-E6.F1.E2.R.E4+\\ E6.F2.E3.R.E4+\frac{1}{4}R^2E4^2E6\end{pmatrix};$$

$C1=8.(E6.E2^2.F1+E3^2.E6.F2-E6.E2.E3.F1).(1+A_1)$;

$F6=4.(E2^2+E3^2-2.E2.E3).E6.(1+A_1)^2$; $F5=2.(-2.E5.F1+E3.F2+E4.R).E1.E8$;

$F4=4.E1.\left(F1.E5-F2.E3-\frac{1}{2}.E4.R\right)-(E3-E5).(4.E1.E8.(1+A_1))$;

$$F3=(E3-E5).(4.E1.(1+A_1)) \; ; \qquad F2=(V_{bi}+V_{ds}).(1+A_1)+(1+A_1).V_{fbf2}+N1 \; ;$$

$$F1=V_{bi}.(1+A_1)+(1+A_1).V_{fbf1}+N1 \; ; \qquad E8=2.\phi_F+(1+A_1).V_{fbf1}-A_1.\left|V_{fbf1}\right|_{y=\frac{t_{si}}{2}}+N1 \; ;$$

$$E6=\exp\left(\frac{-1}{2}\right) ; \qquad E7=\exp\left(\frac{1}{2}\right) ; \qquad N1=\frac{q.N\left(\frac{t_{si}}{2}\right).\lambda_1^{\,2}}{\varepsilon_{si}}$$

$$E5=\exp\left(\frac{L_1+2.L_2}{\lambda_1}\right) ; \qquad E4=1+\exp\left(\frac{2.L_2}{\lambda_1}\right) ; \qquad E3=\exp\left(\frac{L_2}{\lambda_1}\right)$$

$$E2=\exp\left(\frac{-L_1}{\lambda}\right) ; \qquad E1=\exp\left(\frac{L_1+2.L_2}{\lambda_1}\right)-\exp\left(\frac{-L_1}{\lambda_1}\right)$$

where V_{fbf1} , V_{fbf2} and $\left|V_{fbf1}\right|_{y=\frac{t_{si}}{2}}$ are given in equations (2.19) and (2.37)

APPENDIX: E

The drain current is given by

$$I_{ds} = -W.v_n(x).Q_n(x)$$

$$= -W.\sum_{m=1}^{2} v_{nm}(x).Q_{nm}(x)$$

$$= -W.[v_{n1}(x).Q_{n1}(x) + v_{n2}(x).Q_{n2}(x)]$$

$$= -W.\left[\mu_{n1}(x).Q_{n1}(x).\frac{d\phi_{c1}(x)}{dx} + \mu_{n2}(x).Q_{n2}(x).\frac{d\phi_{c2}(x)}{dx}\right]$$

$$= I_1 + I_2 \text{ --- say}$$

where $v_{n1}(x).Q_{n1}(x)$ and $v_{n2}(x).Q_{n2}(x)$ is the velocity and charge of carriers (electrons in this case) in region 1 and region 2 respectively, as shown in the figure below.

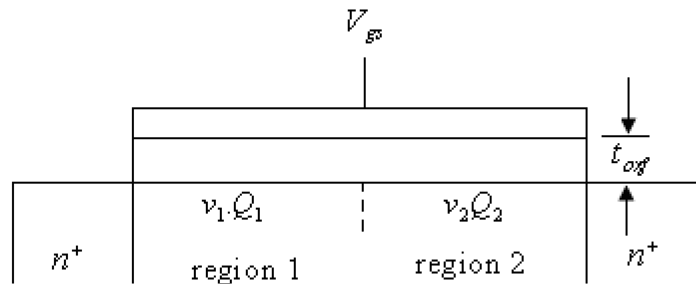


Fig 4.13 n-channel MOSFET structure.